ESD-TR-88-181

Technical Report
812

Microwave Power Amplifier Analysis and Design

L.J. Kushner

16 December 1988

Lincoln Laboratory
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON, MASSACHUSETTS

Prepared for the Department of the Army
under Electronic Systems Division Contract F19628-85-C-0002.

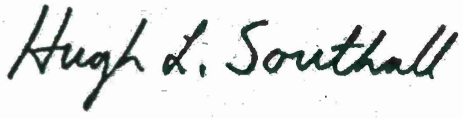
The work reported in this document was performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology, with the support of the Department of the Army under Air Force Contract F19628-85-C-0002.

The views and conclusions contained in this document are those of the contractor and should not be interpreted as necessarily representing the official policies, either expressed or implied, of the United States Government.

The ESD Public Affairs Office has reviewed this report, and it is releasable to the National Technical Information Service, where it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER



Hugh L. Southall, Lt. Col., USAF
Chief, ESD Lincoln Laboratory Project Office

Non-Lincoln Recipients

PLEASE DO NOT RETURN

Permission is given to destroy this document when it is no longer needed.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

MICROWAVE POWER AMPLIFIER ANALYSIS AND DESIGN

L.J. KUSHNER
Group 66

TECHNICAL REPORT 812

16 DECEMBER 1988

LEXINGTON MASSACHUSETTS

ABSTRACT

Output power, efficiency, power dissipation, and optimum load-resistance expressions for idealized microwave Class A and B power amplifiers are derived based on a waveform analysis. The effects of device transconductance variation with bias and circuit harmonic termination are examined. Large-signal gain is determined by calculating the input power needed to produce a given output power. Both closed-form and CAD-based solutions are presented, all based on device dc I-V characteristics and small-signal models. A practical power amplifier design procedure is given and used to design a 22-GHz permeable-based transistor (PBT) power amplifier. Although the analysis and design results presented here are useful by themselves, they are also intended to be used in conjunction with other CAD and measurement techniques (such as harmonic balance and load pull) to arrive at a starting point. Device designers also should find these results useful, allowing them to predict how changes in device parameters will affect microwave power amplifier performance.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

ACKNOWLEDGMENTS

This work grew out of discussions with Mark Hollis, Rick Mathews, Al Murphy, Carl Bozler, and Kirby Nichols in our search for better PBTs. Discussions with Bill Courtney were most helpful, and his research was the basis for the gain calculations of Section 3. The author would like to thank Dave Snider and Ron Bauer for their interest in this work and for providing the time needed to complete it.

MICROWAVE POWER AMPLIFIER ANALYSIS AND DESIGN

1. INTRODUCTION

Given the variety of microwave nonlinear computer-aided design (CAD) programs available today, such as the time-domain program SPICE (developed at the University of California, Berkeley), and the harmonic-balance programs Libra (EEsof, Inc.) and Microwave Harmonica (Compact Software), one might wonder what good are the relatively simplistic, quasi-static results presented in this report. Assuming that the device in question can adequately fit into their models, one would expect these other more complex analysis methods to provide more accurate results. Unlike the methods presented here, these nonlinear-CAD programs can be used to calculate intermodulation performance. However, while great for analysis, these computation-intensive numeric methods provide little insight needed for design. They provide specific results for a given device, but do not show general trends and relationships. In contrast, the results presented in this report are more general, giving a better picture of amplifier operation while requiring far fewer calculations.

Using most CAD programs, designing a circuit is accomplished by repeatedly reanalyzing it after varying some circuit-element values, a procedure usually referred to as "optimization." The better the designer's first guess (initial value), the fewer parameters that are varied, and the more constrained these parameters are, the faster these programs converge to an optimum solution. While important for linear-CAD optimization, a good first guess becomes critical in nonlinear-CAD, due to the required order-of-magnitude increase in computation. The results presented in this report provide a fast and simple method of attaining that all-important initial value, much closer to the ultimate solution than would be obtained by small-signal analysis or by celestial extraction (i.e., pulling numbers out of the air).

The methods presented are sufficient to design many power amplifiers without the need for any additional nonlinear-CAD analysis. Several other power amplifier applications, such as load-pull measurements and empirical amplifier tuning, also benefit from these results. Besides providing a starting point by estimating the output power and gain obtainable from an amplifier, this method also tells you when to stop.

Rather than a numeric-based method, the procedures described below are based primarily on analytical expressions and graphical techniques, leading to better understanding and insight. How a certain parameter will affect amplifier performance is obvious from the derived equations, rather than requiring a whole battery of computer runs. A device designer can use these results to quickly predict the microwave power performance obtainable from a device, rather than waiting for circuit design, fabrication, and test.

Output power, efficiency, power dissipation, and optimum load-resistance results are derived in Section 2 based on a waveform analysis. These are essentially the textbook Class A and B power amplifier results for two different device types (constant or linear transconductance) and

two different load circuits (resistive or tuned). Unfortunately, no textbook known to the author covers more than just a few of the simplest cases. (The most complete coverage appears in [1], but this covers just a small subset of the cases presented here.) The derivations presented below attempt to fill this void. All these results are consolidated into three tables for easy reference.

Section 3 combines the output power calculation of Section 2 with an input power calculation to arrive at large-signal gain. Although extended considerably, the basic idea for this gain calculation method came from Courtney and Gopinath [2] who derive some of the same output power and efficiency results presented here, but from a somewhat different approach. Analytical expressions for input power are derived in terms of the device parameters, followed by a novel numeric method of input power calculation employing a linear circuit analysis program, such as Super-Compact (Compact Software). This simple, yet accurate analysis method is probably the most important contribution of this report.

Section 4 pulls all the pieces together and comes up with a straightforward power amplifier design procedure. This method has been used to design a variety of 22-GHz PBT power amplifiers (70 to 400 mW) with excellent correlation between predicted and measured responses. One such amplifier design is given as an example.

It should be pointed out that many of the derivations below assume a voltage-controlled device such as an FET, PBT, or HEMT and would have to be modified somewhat to handle current-controlled devices, such as bipolar transistors.

2. OUTPUT POWER AND EFFICIENCY CALCULATIONS

In this section, the output power, drain efficiency, power dissipation, and optimum load resistance (for maximum output power) are calculated for Class A and B power amplifiers based on a waveform analysis and a device's static I-V characteristics While most textbooks derive these results for devices with a constant-transconductance (g_m) versus gate-voltage characteristic [Figure 2-1(a)], most real-life devices (such as FETs and PBTs) tend to have control characteristics more closely approximated by a linear-transconductance variation [Figure 2-1(b)]. Furthermore, all the textbook derivations assume a perfect tuned-load circuit [Figure 2-2(b)], while in practice, few microwave amplifiers provide a short circuit to all the harmonic frequencies. These issues are not just theoretical, but have practical implications. Some FET designers have intentionally modified their device doping profiles in an effort to get constant rather than linear-transconductance devices [3], claiming improved output power, gain, and efficiency. Concerning the harmonic termination issue, power amplifier designers should know what penalty they will pay for failing to properly terminate amplifier harmonic frequencies.

The analysis presented derives results for Class A and B amplifiers, with either constant- or linear-g_m devices, and with resistive or tuned loads (see Figure 2-2). Note that in all cases, the dc bias to the device is assumed to be brought into the circuit through large dc chokes, and blocked from the load by large coupling capacitors. Besides these simple load types, the basic derivations allow a broader range of load impedances to be evaluated. While infinite device output impedance (i.e., flat I-V curves) is assumed for the initial derivations, Section 3 considers the effect of finite output impedance.

2.1 Current Waveforms

Figure 2-3 contains the input voltage waveforms (v_{GS}), device control characteristics, output current waveforms (i_{DS}), load-lines*, and output voltage waveforms for all the cases considered. For now, only the input voltage and output currents will be discussed. Output voltages and load-lines are addressed later, but are included in this figure for completeness.

As illustrated in Figure 2-3, using the idealized device control characteristics along with sinusoidal gate-voltage excitations of proper amplitude and offset, device drain currents can be determined for each of the four combinations of transconductance type (constant or linear) and amplifier class (A or B). Notice that i_{DS} is assumed to be independent of v_{DS}, which from Figure 2-1 is seen to be true as long as v_{DS} stays above V_{SAT} and below the device breakdown voltage (V_{BR}).† If the device output impedance were finite rather than infinite as assumed, i_{DS} would be dependent on v_{DS}, greatly complicating this analysis.

---

* A plot of the instantaneous drain-source current versus voltage superimposed on the device I-V characteristics.

† More precisely, it is actually the drain-gate voltage that must stay below V_{BR}, but since the gate-source voltage is usually small, $v_{DS} \simeq v_{DG}$ and the previous statement is approximately correct. This analysis assumes that when the device is pinched-off, drain-gate breakdown is determined solely by the drain-gate voltage, as suggested by Tajima and Miller [4]. Breakdown limitations are discussed in greater detail in Section 2.2.

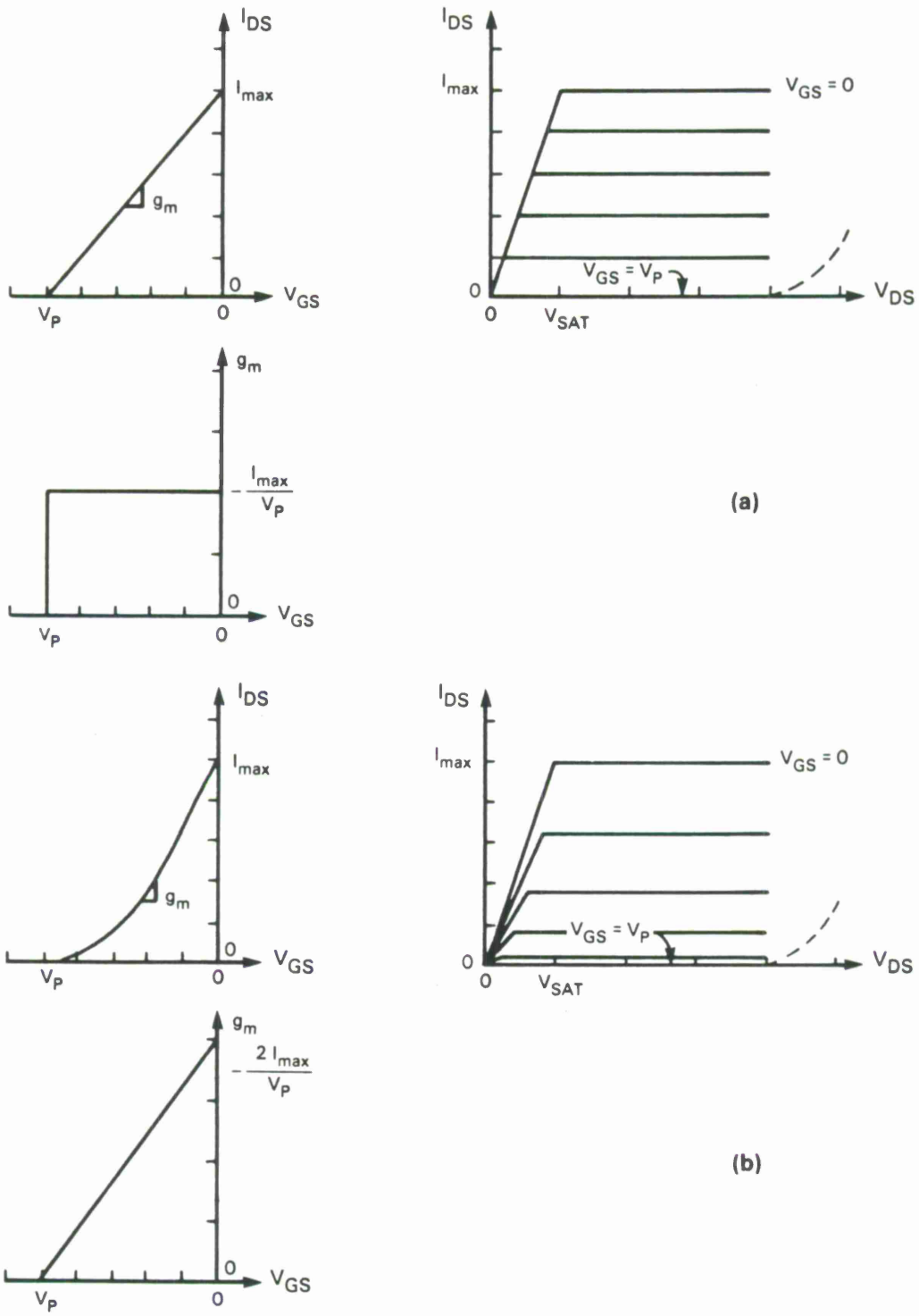


Figure 2-1. Device characteristics: (a) constant- and (b) linear-g_m devices.

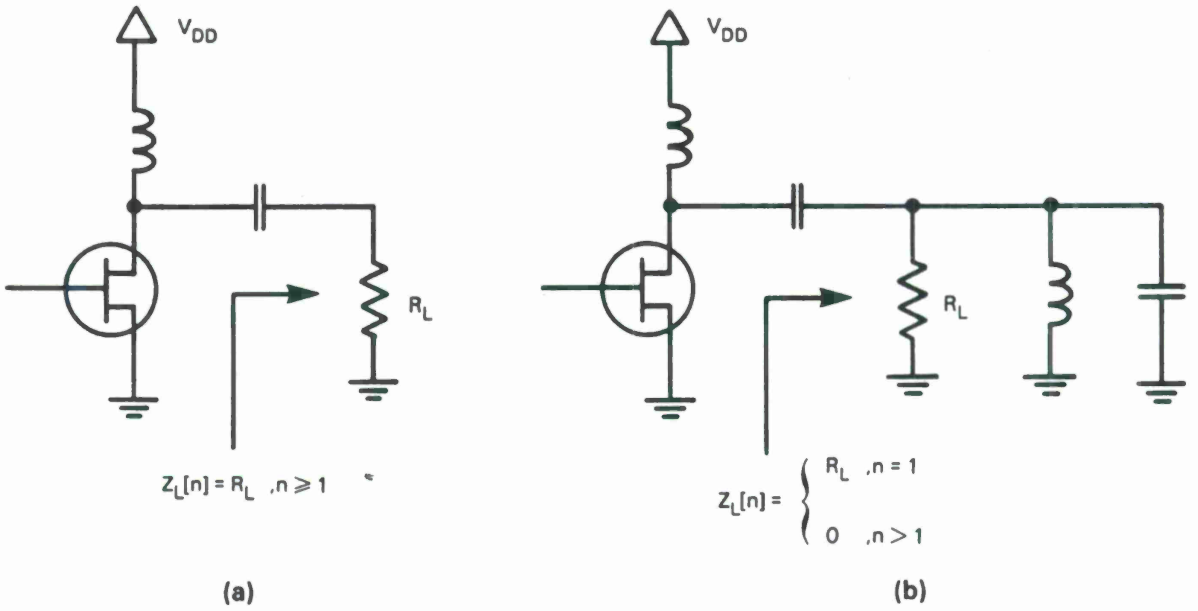


Figure 2-2. Load circuits: (a) resistive and (b) tuned loads.

Two important observations can be made concerning the current waveforms of Figure 2-3. Looking at these drain-source currents for the first time, it is somewhat surprising to see how similar the waveforms are, given that the Class B amplifier only conducts current during half the rf input cycle, while the Class A amplifier conducts during the entire cycle. Current waveforms for an amplifier operating Class AB lie somewhere between these Class A and Class B currents. A more dramatic difference between Class A and B appears in the input (gate-to-source voltage) waveforms. Class B operation requires twice the drive-voltage swing as Class A, resulting in ~6 dB less rf gain. (In reality, gain in Class B operation is not a full 6 dB worse than in Class A, due to the reduced input capacitance at this bias point, and finite device output-impedance.)

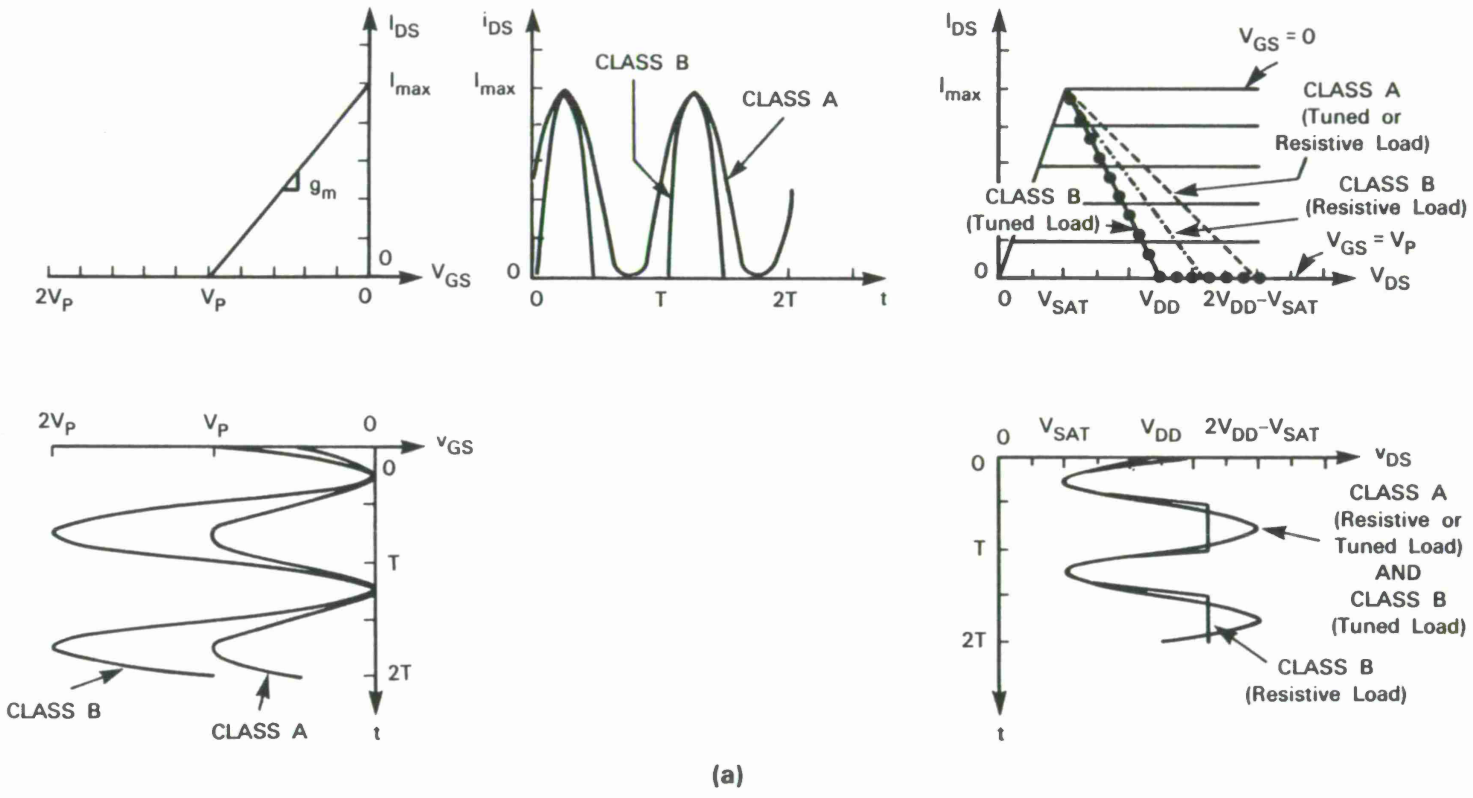
Analytic expressions for the current waveforms of Figure 2-3 are easily obtained for each of the four cases:

Class A, constant g_m:
$$i_{DS1} = (I_{max}/2)\,(1 + \sin \omega_o t) \qquad ,0 \leq t \leq T \qquad (2.1)$$

Class A, linear g_m:
$$i_{DS2} = (I_{max}/4)\,(1 + \sin \omega_o t)^2 \qquad ,0 \leq t \leq T \qquad (2.2)$$

Class B, constant g_m:
$$i_{DS3} = \begin{cases} I_{max} \sin \omega_o t & ,0 \leq t \leq T/2 \\ 0 & ,T/2 \leq t \leq T \end{cases} \qquad (2.3)$$

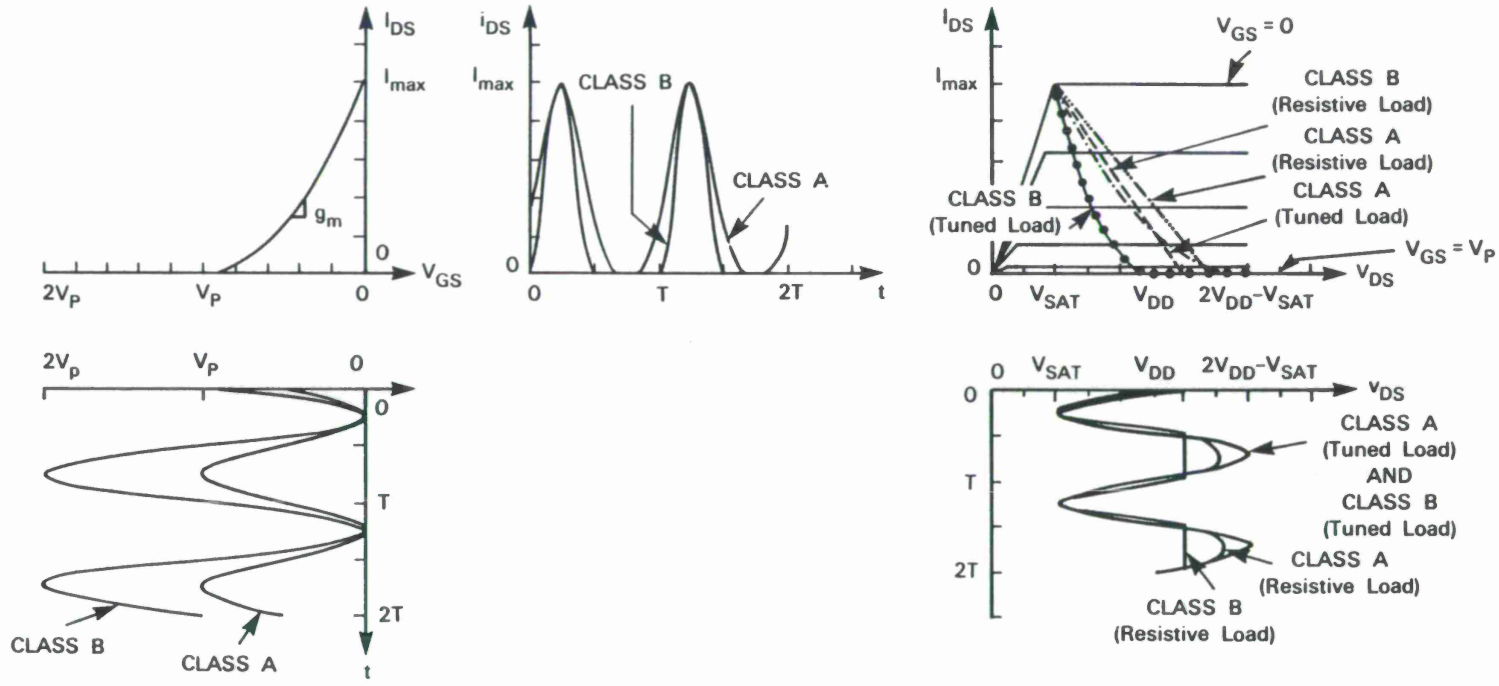
Class B, linear g_m:
$$i_{DS4} = \begin{cases} I_{max} \sin^2 \omega_o t & ,0 \leq t \leq T/2 \\ 0 & ,T/2 \leq t \leq T \end{cases} \qquad (2.4)$$



(a)

Figure 2-3(a). Amplifier waveforms: constant-g_m devices.

103225-3



(b)

Figure 2-3(b). Amplifier waveforms: linear-g_m devices.

Being periodic, each of these waveforms can be expressed as a Fourier series

$$i_{DS}(t) = \sum_{n=-\infty}^{n=\infty} I_{DS}[n]\, e^{jn\omega_o t} \quad . \tag{2.5}$$

A Fourier analysis was performed on these four current waveforms to determine how much current flows at each harmonic frequency (Table 2-1). The fundamental component of drain-source current, $I_{DS}[1]$, is the same for Class A (both cases 1 and 2) and Class B/constant g_m (case 3), but is 1.4 dB lower in the class B/linear g_m (case 4). Although the current waveforms of these first three cases have the same fundamental component, significant differences occur in their harmonic contents.

TABLE 2-1

Fourier Analysis of Drain-Source-Current Waveforms

CASE	g_m TYPE	Drain-Source-Current Fourier Components				
		$I_{DS}[0]$	$I_{DS}[1]$	$I_{DS}[2]$	$I_{DS}[n_{odd} \neq 1]$	$I_{DS}[n_{even} \neq 2]$
CLASS A						
1	Constant	$\frac{I_{max}}{2}$	$\frac{I_{max}}{4j}$	0	0	0
2	Linear	$\frac{3I_{max}}{8}$	$\frac{I_{max}}{4j}$	$-\frac{I_{max}}{16}$	0	0
CLASS B						
3	Constant	$\frac{I_{max}}{\pi}$	$\frac{I_{max}}{4j}$	$-\frac{I_{max}}{3\pi}$	0	$\frac{I_{max}}{\pi(1-n^2)}$
4	Linear	$\frac{I_{max}}{4}$	$\frac{2I_{max}}{3\pi j}$	$-\frac{I_{max}}{8}$	$\frac{2I_{max}}{j\pi n(4-n^2)}$	0

2.2 Voltage Waveforms, Output Power, Efficiency, Power Dissipation, and Load Resistance

The current waveforms and Fourier analysis of Section 2.1 can be combined with the load circuits of Figure 2-2 to produce the drain-to-source voltage frequency components, $V_{DS}[n]$, and time waveforms, $v_{DS}(t)$:

$$V_{DS}[n] = \begin{cases} V_{DD} & ,n = 0 \\ -I_{DS}[n]\, Z_L[n] & ,n \geq 1 \end{cases} \tag{2.6}$$

and

$$v_{DS}(t) = \sum_{n=-\infty}^{n=\infty} V_{DS}[n]\, e^{jn\omega_o t} \quad . \tag{2.7}$$

Notice that Equation (2.6) allows arbitrary load impedances to be connected to the device. This can lead to erroneous conclusions, however, since this result was derived by assuming that the device drain-to-source voltage v_{DS} stays between V_{SAT} and approximately V_{BR}, keeping the drain-to-source current i_{DS} independent of v_{DS}. While this will be true for small load impedances, large-impedance loads will cause v_{DS} to swing beyond this region, violating the initial assumption. In particular, the optimum (for maximum output power) fundamental frequency load resistance is selected just large enough so that the device operation swings from saturation to the verge of breakdown. Any larger resistance will cause voltage clipping not modeled by this frequency domain analysis. This issue is discussed in greater detail below.

Equation (2.6) requires that the load impedance $Z_L[n]$ be known before $V_{DS}[n]$ can be determined. To choose the proper load impedance for maximum output power, a digression to discuss output power and load-lines is in order.

The power dissipated by the device can be found in either the time or frequency domains. In the time domain

$$P_{DISS} = \frac{1}{T} \int_0^T i_{DS}(t)\, v_{DS}(t)\, dt \quad . \tag{2.8}$$

By plugging the Fourier series expansions for $i_{DS}(t)$ and $v_{DS}(t)$ [Equations (2.5) and (2.7)] into Equation (2.8) or by using Parseval's Theorem, the dissipated power can also be computed from the frequency domain components

$$P_{DISS} = \sum_{n=-\infty}^{n=\infty} I_{DS}[n]\, V^*_{DS}[n] \quad . \tag{2.9}$$

Since $i_{DS}(t)$ and $v_{DS}(t)$ are real time functions, $I_{DS}[n]$ and $V_{DS}[n]$ are conjugate symmetric, so Equation (2.9) can be rewritten as:

$$P_{DISS} = \sum_{n=0}^{n=\infty} P_{DISS}[m] \tag{2.10}$$

where

$$P_{DISS}[m] = \begin{cases} I_{DS}[0]\ V_{DS}[0] & ,m = 0 \\ 2\ \mathrm{Re}\ \ I_{DS}[m]\ V^{*}_{DS}[m] & ,m \geq 1 \end{cases} .$$

In Equation (2.10), $V_{DS}[0]$ is the supply voltage V_{DD}, while $I_{DS}[0]$ is the time average value of the $i_{DS}(t)$ waveform as determined by the device bias point, the input signal drive level, and the waveform shape. If the device delivers, rather than dissipates, power at a frequency $m\omega_o$, $P_{DISS}[m] < 0$, and the output power at that frequency is given by

$$P_{out}[m] = -P_{DISS}[m] = -2\ \mathrm{Re}\ \{I_{DS}[m]\ V^{*}_{DS}[m]\} \qquad ,m \geq 1 \quad . \tag{2.11}$$

In order to maximize output power, the phases of $V_{DS}[m]$ and $I_{DS}[m]$ are made 180° apart, reducing the expression for $P_{out}[m]$ to

$$P_{out}[m] = 2\ |I_{DS}[m]|\ |V_{DS}[m]|, \text{ for } \angle I_{DS}[m] - \angle V_{DS}[m] = 180° \qquad ,m \geq 1 \quad . \tag{2.12}$$

From Equation (2.12), it is obvious that $P_{out}[m]$ is further maximized by maximizing the magnitudes of $I_{DS}[m]$ and $V_{DS}[m]$. For the device without parasitics considered to this point, the 180° phase condition is met by using a purely real (i.e., no reactive component) load impedance R_L, and the magnitude condition is met by choosing the optimum load-line, as illustrated in Figure 2-4 (for the simple constant g_m, Class A amplifier case). By choosing the load-line to go through the points (V_{SAT}, I_{max}) and $(2V_{DD} - V_{SAT}, 0)$, voltage swing ΔV and current swing ΔI are both maximized for a given supply voltage, V_{DD}. This load-line is traversed by biasing the device at $(V_{DD}, I_{max}/2)$ and by setting R_L equal to $\Delta V/\Delta I = 2(V_{DD} - V_{SAT})/I_{max} \equiv R_{Lopt}$. Choosing $R_L < R_{Lopt}$ results in the same current swing [Figure 2-4(b)], but reduced voltage swing [Figure 2-4(c)], while choosing $R_L > R_{Lopt}$ results in approximately the same voltage swing (assuming $2V_{DD} - V_{SAT} \simeq V_{BR}$), but reduced current swing. In other words, by picking the load-line to simultaneously maximize both ΔV and ΔI, output power is maximized.† This explains why a load circuit designed for maximum small-signal gain almost always results in suboptimal power performance. In order to achieve maximum small-signal gain, R_L is chosen to be equal to the device incremental output resistance which, in general, is much larger than R_{Lopt} (especially for a high-current power device). This choice of R_L results in the full voltage swing, $\Delta V \simeq V_{BR} - V_{SAT}$, but ΔI much less than I_{max}.

---

† An interesting argument can be made concerning the choice or R_L. If R_L is increased beyond R_{Lopt}, $v_{DS}(t)$ begins to become clipped, but its fundamental component $V_{DS}^{[1]}$ continues to increase beyond that obtained when $R_L = R_{Lopt}$. Meanwhile, $I_{DS}^{[1]}$ begins to decrease. If $I_{DS}^{[1]}$ could somehow be kept from dropping faster than $V_{DS}^{[1]}$ increases, output power would continue to increase as R_L is increased beyond R_{Lopt}. While further discussion is beyond the scope of this report, the reader is referred to [5] and [6] for more details.

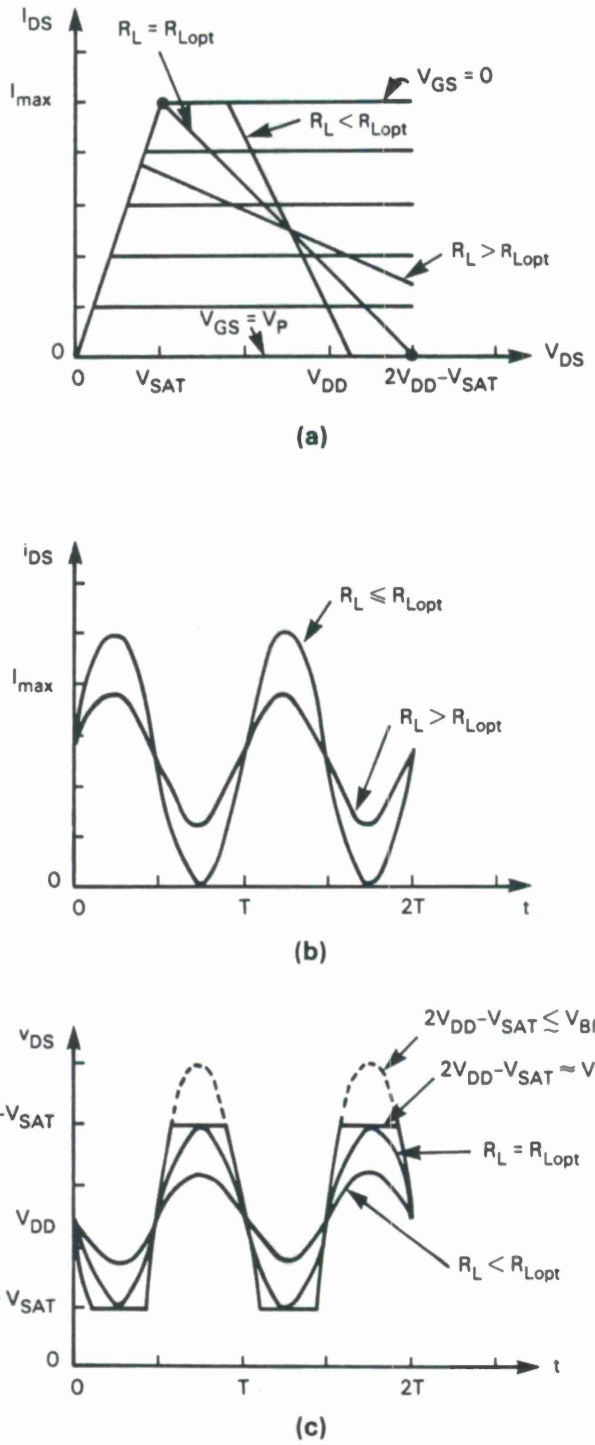


Figure 2-4. (a) Load-line selection, (b) effect on drain-source current, and (c) voltage.

While Equations (2.10) through (2.12) are quite useful in picking the load resistance, for further calculations it is more convenient to express power in terms of current and load impedance rather then current and voltage. From Equation (2.6), $V_{DS}[n] = -I_{DS}[n]\ Z_L[n]$ for $n \geq 1$, and assuming that $Z_L[n]$ is conjugate symmetric, Equation (2.9) can be rewritten as

$$P_{DISS} = I_{DS}[0]\ V_{DS}[0] - 2 \sum_{n=0}^{n=\infty} |I_{DS}[n]|^2\ \mathrm{Re}\ \{Z_L[n]\} \quad . \tag{2.13}$$

This expression is the dc power into the device minus the sum of the ac powers delivered to the load, i.e.,

$$P_{DISS} = P_{DC} - \sum_{n=0}^{n=\infty} P_{out}[n] \tag{2.14a}$$

where

$$P_{DC} = I_{DS}[0]\ V_{DD} \tag{2.14b}$$

and

$$P_{out}[n] = 2\,|I_{DS}[n]|^2\ \mathrm{Re}\ \{Z_L[n]\} \tag{2.14c}$$

$$= \text{power delivered to load at } n^{th} \text{ harmonic} \quad .$$

Before leaving the subject of output power, two definitions are given:

$$\text{drain efficiency} \equiv \eta_D = P_{out}[1]/P_{DC} \tag{2.15}$$

$$\text{power-added efficiency} \equiv \eta_{add} = \eta_D\ (1 - 1/G) \quad . \tag{2.16}$$

The term "G" in Equation (2.16) is large-signal gain of the amplifier. Notice that $\eta_{add} \leq \eta_D$, with equality being approaches in the limit as G approaches infinity. Since Section 3 is devoted to the calculation of large-signal gain, G will not be discussed further here.

Having determined that output power is maximized by selecting the load resistance to maximize both current and voltage swings, the output-voltage waveforms can now be determined, along with expressions for output power (at the fundamental and harmonic frequencies), power dissipation, drain efficiency, and optimum load resistance:

(1) $i_{DS}(t)$ and $I_{DS}[n]$ are determined from Equations (2.1) through (2.4) and Table 2-1, respectively, once the amplifier Class (A or B) and transconductance variation (constant or linear) have been selected. It is assumed that $R_L \leq R_{Lopt}$, so current swing is at its maximum.

(2) Analytical expressions for $V_{DS}[n]$ in terms of $Z_L[n]$ are determined from Equation (2.6).

(3) $v_{DS}(t)$ is obtained from Equation (2.7).

(4) R_L is chosen so that the minimum value of $v_{DS}(t)$ is equal to V_{SAT}. This provides the maximum possible voltage swing for a given supply voltage and waveform shape, assuming the device is operating below breakdown. Since maximum current swing was already assumed, this value of R_L corresponds to R_{Lopt}, giving maximum output power.

(5) Output power (fundamental and harmonics) and dissipated power are calculated from Equations (2.14c) and (2.14a), respectively.

(6) Drain efficiency is determined from Equation (2.15).

The above procedure was used to analyze Class A and B amplifiers with either constant- or linear-transconductance devices, and with resistive or tuned loads. The results of this analysis are given in Table 2-2. While the above procedure goes from the time domain $i_{DS}(t)$ to the frequency domain $I_{DS}[n]$ and $V_{DS}[n]$ and back to the time-domain $v_{DS}(t)$, the same results can be obtained by an alternative equivalent method for the case of these simple resistive and tuned loads. Due to the simple nature of the loads considered, the form of the time-domain voltage $v_{DS}(t)$ can be determined by inspection, and the frequency-domain components $V_{DS}[n]$ can be obtained by a Fourier analysis of $v_{DS}(t)$. However, any load circuit more complex than a resistive or tuned load cannot easily be handled by this alternative method, while the procedure detailed above has no problem handling more general load impedances.

Several important observations can be made from Table 2-2:

(1) In all cases, drain efficiency is degraded by the term $\alpha = (V_{DD} - V_{SAT})/V_{DD}$. Clearly, the larger the supply voltage V_{DD} is relative to the saturation voltage V_{SAT} the better the efficiency. Unfortunately, V_{DD} cannot be increased without limit due to drain-gate breakdown, excessive power dissipation in the device, and gain reduction at higher operating voltages. These issues are discussed in more detail below.

(2) For Class A operation, linear- rather than constant-g_m is preferable, as long as a tuned load can be implemented. In this case (2b), output power remains the same as in the constant-g_m device, but drain efficiency improves from 50 to 67 percent. Terminating the harmonics resistively (cases 1a and 2a) rather than shorting them to ground (cases 1b and 2b) results in a decrease in both output-power and efficiency for the linear-g_m device, but has no effect on the constant-g_m device (as expected, since in cases 1a and 1b, no harmonics are generated).

(3) In Class B operation, better output power is achieved with constant- than with linear-g_m devices, for both resistive and tuned loads (cases 3a versus 4a and cases 3b versus 4b). This makes sense, since in a constant-g_m device, high device gain is maintained all the way down to pinch-off, whereas in a linear-g_m device, gain drops to zero as gate-to-source voltage approaches pinch-off (V_P). Being biased at V_P, a large fraction of the Class B input cycle occurs in this low-gain (for linear-g_m) region.

TABLE 2-2

Class A and B Power Amplifier Performance ($V_{DD} < V_{DDmax}$)

CASE	g_m TYPE	LOAD[1] TYPE	R_{Lopt}[2] (Ω)	V_{DSmax} (V)	P_{DISS} (W)	η_D[3] (%)	P_{out}[4] (W)	P_{out} (Relative) (dB)
CLASS A								
1a	Constant	Resistive	$2\frac{(V_{DD}-V_{SAT})}{I_{max}}$	$V_{DD}+(V_{DD}-V_{SAT})$	$\frac{(V_{DD}+V_{SAT})I_{max}}{4}$	50α	$\frac{(V_{DD}-V_{SAT})I_{max}}{4}$	0
1b	Constant	Tuned	$2\frac{(V_{DD}-V_{SAT})}{I_{max}}$	$V_{DD}+(V_{DD}-V_{SAT})$	$\frac{(V_{DD}+V_{SAT})I_{max}}{4}$	50α	$\frac{(V_{DD}-V_{SAT})I_{max}}{4}$	0
2a	Linear	Resistive	$\frac{8}{5}\frac{(V_{DD}-V_{SAT})}{I_{max}}$	$V_{DD}+\frac{3}{5}(V_{DD}-V_{SAT})$	$\frac{(0.65V_{DD}+0.85V_{SAT})I_{max}}{4}$	53α	$\frac{(V_{DD}-V_{SAT})I_{max}}{5}$	-0.97
2b	Linear	Tuned	$2\frac{(V_{DD}-V_{SAT})}{I_{max}}$	$V_{DD}+(V_{DD}-V_{SAT})$	$\frac{(0.5V_{DD}+V_{SAT})I_{max}}{4}$	67α	$\frac{(V_{DD}-V_{SAT})I_{max}}{4}$	0
CLASS B								
3a	Constant	Resistive	$\frac{\pi}{\pi-1}\frac{(V_{DD}-V_{SAT})}{I_{max}}$	$V_{DD}+\frac{1}{\pi-1}(V_{DD}-V_{SAT})$	$\frac{(0.4V_{DD}+0.87V_{SAT})I_{max}}{4}$	58α	$\frac{\pi(V_{DD}-V_{SAT})I_{max}}{8(\pi-1)}$	-1.3
3b	Constant	Tuned	$2\frac{(V_{DD}-V_{SAT})}{I_{max}}$	$V_{DD}+(V_{DD}-V_{SAT})$	$\frac{(0.27V_{DD}+V_{SAT})I_{max}}{4}$	79α	$\frac{(V_{DD}-V_{SAT})I_{max}}{4}$	0
4a	Linear	Resistive	$\frac{4}{3}\frac{(V_{DD}-V_{SAT})}{I_{max}}$	$V_{DD}+\frac{1}{3}(V_{DD}-V_{SAT})$	$\frac{(0.33V_{DD}+0.66V_{SAT})I_{max}}{4}$	48α	$\frac{32(V_{DD}-V_{SAT})I_{max}}{27\pi^2}$	-3.2
4b	Linear	Tuned	$\frac{3\pi}{4}\frac{(V_{DD}-V_{SAT})}{I_{max}}$	$V_{DD}+(V_{DD}-V_{SAT})$	$\frac{(0.15V_{DD}+0.85V_{SAT})I_{max}}{4}$	85α	$\frac{2(V_{DD}-V_{SAT})I_{max}}{3\pi}$	-0.71

1. Resistive load: $Z_L[n] = R_{Lopt}$, $n \geq 1$

   Tuned load: $Z_L[n] = \begin{cases} R_{Lopt}, & n = 1 \\ 0, & n > 1 \end{cases}$

2. R_{Lopt} chosen so that $V_{DSmin} = V_{SAT}$

3. $\alpha = \frac{(V_{DD}-V_{SAT})}{V_{DD}}$

4. Fundamental frequency output power

(4) Looking at drain efficiency in Class B operation, the linear-g_m device has an apparent edge if a tuned circuit is used (85 versus 79 percent), while the constant-g_m device wins out if a resistive load is used (58 versus 48 percent). In low-gain devices, the apparent efficiency edge of the linear-g_m/tuned-load amplifier may be negated by its decreased gain (-0.71 dB) when η_{add}, rather than η_D, is calculated.

(5) In all cases, a tuned load is superior to a resistive load. This makes sense, since by shorting any harmonic current to ground, the tuned circuit prevents any power from being dissipated at these harmonic frequencies. Note that a tuned load is the type always assumed in the textbook derivations of these efficiency expressions. While nice in theory, providing a short circuit to all the harmonics "down inside" the device (i.e., back before any device output parasitics) may be difficult to implement. This is one case when the millimeter-wave designers have it easy — usually C_{ds} is large enough at these frequencies to short-out most of the higher-order harmonics.

(6) While R_{Lopt} does vary from case to case, the variation is not as large as one might think. The greatest variation is in the Class B/linear-g_m cases (4a and 4b), going from $1.33(V_{DD} - V_{SAT})/I_{max}$ to $2.36(V_{DD} - V_{SAT})/I_{max}$ — less than a 2-to-1 variation. Note that cases 1a, 1b, 2b, and 3b all have the textbook value of R_{Lopt} equal to $2(V_{DD} - V_{SAT})/I_{max}$.

All the results in Table 2-2 assume that the voltage $v_{DS}(t)$ is never large enough to cause drain-gate breakdown. Assuming that the device can handle the added power dissipation and can still continue to provide adequate gain at higher drain voltages, the supply voltage V_{DD} and load resistance R_L can both be increased until the peak swing of the drain-gate voltage approaches the breakdown voltage, V_{BR}. At this point, ΔI and ΔV will both be at their maximum possible values, resulting in maximum output power. This breakdown point can be easily determined from the device drain-gate breakdown voltage V_{BR}, the peak (i.e., most positive) value of $v_{DS}(t)$, V_{DSmax}, the minimum (i.e., most negative) value of $v_{GS}(t)$, V_{GSmin}, and the waveshapes

$$v_{DG}(t) = v_{DS}(t) - v_{GS}(t) \tag{2.17}$$

$$V_{DGmax} = V_{DSmax} - V_{GSmin} \tag{2.18}$$

Equation (2.18) assumes that V_{DSmax} and V_{GSmin} occur simultaneously, which will be the case for all the amplifiers considered here. V_{GSmin} can be easily determined from the gate-voltage waveforms in Figure 2-3. For Class A operation, $V_{GSmin} = V_P$, while in Class B, $V_{GSmin} = 2\ V_P$. V_{DSmax} is determined on a case-by-case basis from the $v_{DS}(t)$ waveforms. In order to keep the drain-gate junction from breaking down, V_{DGmax} must be kept below V_{BR}. Using these relationships to determine the maximum-allowed supply voltage V_{DDmax}, the results of Table 2-2 can be modified by replacing V_{DD} with V_{DDmax}, to give the performance obtainable from these idealized amplifiers at the maximum possible output-power point (Table 2-3). Remember, these results assume that the device can handle the power dissipation, which may not always be the case.

TABLE 2-3

Class A and B Power Amplifier Performance ($V_{DD} = V_{DDmax}$)

CASE	g_m TYPE	LOAD[1] TYPE	R_{Lopt}[2,3] (Ω)	V_{DDmax} (V)	P_{DISS} (W)	η_D[4] (%)	P_{out}[5] (W)	P_{out}[6] (Relative) (dB)
CLASS A								
1a	Constant	Resistive	$\frac{V_A}{I_{max}}$	$\frac{1}{2}(V_{BR} + V_P + V_{SAT})$	$0.12(V_{BR} + V_P)I_{max} + 0.38\,V_{SAT}I_{max}$	50α	$\frac{V_A I_{max}}{8}$	0
1b	Constant	Tuned	$\frac{V_A}{I_{max}}$	$\frac{1}{2}(V_{BR} + V_P + V_{SAT})$	$0.12(V_{BR} + V_P)I_{max} + 0.38\,V_{SAT}I_{max}$	50α	$\frac{V_A I_{max}}{8}$	0
2a	Linear	Resistive	$\frac{V_A}{I_{max}}$	$\frac{5}{8}(V_{BR} + V_P + \frac{3}{5}V_{SAT})$	$0.10(V_{BR} + V_P)I_{max} + 0.27\,V_{SAT}I_{max}$	53α	$\frac{V_A I_{max}}{8}$	0
2b	Linear	Tuned	$\frac{V_A}{I_{max}}$	$\frac{1}{2}(V_{BR} + V_P + V_{SAT})$	$0.063(V_{BR} + V_P)I_{max} + 0.31\,V_{SAT}I_{max}$	67α	$\frac{V_A I_{max}}{8}$	0
CLASS B								
3a	Constant	Resistive	$\frac{V_B}{I_{max}}$	$1 - \frac{1}{\pi}\,V_{BR} + 2V_P + \frac{V_{SAT}}{\pi - 1}$	$0.07(V_{BR} + 2V_P)I_{max} + 0.25\,V_{SAT}I_{max}$	58α	$\frac{V_B I_{max}}{8}$	0
3b	Constant	Tuned	$\frac{V_B}{I_{max}}$	$\frac{1}{2}(V_{BR} + 2V_P + V_{SAT})$	$0.03(V_{BR} + 2V_P)I_{max} + 0.28\,V_{SAT}I_{max}$	79α	$\frac{V_B I_{max}}{8}$	0
4a	Linear	Resistive	$\frac{V_B}{I_{max}}$	$\frac{3}{4}(V_{BR} + 2V_P + \frac{1}{3}V_{SAT})$	$0.06(V_{BR} + 2V_P)I_{max} + 0.19\,V_{SAT}I_{max}$	48α	$\frac{8V_B I_{max}}{9\pi^2}$	-1.4
4b	Linear	Tuned	$\frac{3\pi V_B}{8I_{max}}$	$\frac{1}{2}(V_{BR} + 2V_P + V_{SAT})$	$0.02(V_{BR} + 2V_P)I_{max} + 0.23\,V_{SAT}I_{max}$	85α	$\frac{V_B I_{max}}{3\pi}$	-0.71

1. Resistive load: $Z_L[n] = R_{Lopt}$, $n \geq 1$

   Tuned load: $Z_L[n] = \begin{cases} R_{Lopt}, & n = 1 \\ 0, & n > 1 \end{cases}$

2. R_{Lopt} chosen so that $V_{DSmin} = V_{SAT}$
3. $V_A = V_{BR} + V_P - V_{SAT}$; $V_B = V_{BR} + 2V_P - V_{SAT}$
4. $\alpha = \frac{(V_{DD} - V_{SAT})}{V_{DD}}$
5. Fundamental frequency output power
6. Calculated assuming $V_P \simeq 0$

Several comments and observations should be made regarding the results in Table 2-3:

(1) The output power obtained from the resistively terminated amplifiers [all the (a) cases] improved relative to the comparable values in Table 2-2. In Table 2-2, all the amplifiers had the same supply voltage V_{DD}, whereas in Table 2-3 the supply voltages are set equal to V_{DDmax}, which is different dependent upon the case. This arises due to the various drain-source voltage waveforms (Figure 2-3). The resistively terminated circuit drain-source-voltage waveforms, $v_{DS}(t)$, have a smaller peak-to-average ratio than in the tuned-load cases, so V_{DD} can be increased without drain-gate breakdown occurring.

(2) The entries in the P_{out} (relative) column in Table 2-3 were calculated assuming $V_P \simeq 0$. Looking at the previous column labeled "P_{out} (W)," if $V_P < 0$, then the maximum power output in Class B is less than that obtained in Class A, by the ratio V_B/V_A. The more negative V_P is, the lower this ratio. This is the argument made by Lane and Hahn [7] in favor of small $|V_P|$. It should be pointed out that these arguments only apply when operating the device right up on the verge of drain-gate breakdown, as done in Table 2-3, but not at lower operating voltages.

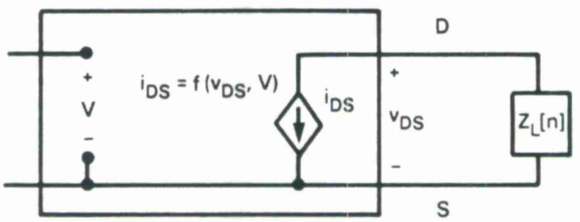
(3) All the other conclusions from Table 2-2 concerning VSAT, constant versus linear g_m, and tuned versus resistive loads still apply to the results in Table 2-3. V_{SAT} should be minimized, tuned loads are better than (or equal to) resistive loads, linear-g_m devices are superior in Class A operation and constant-g_m devices are usually preferable in Class B. Besides their higher output-power and gain in Class B operation, constant-g_m devices are more linear, resulting in better unsaturated performance and less intermodulation distortion.

3. LARGE-SIGNAL GAIN

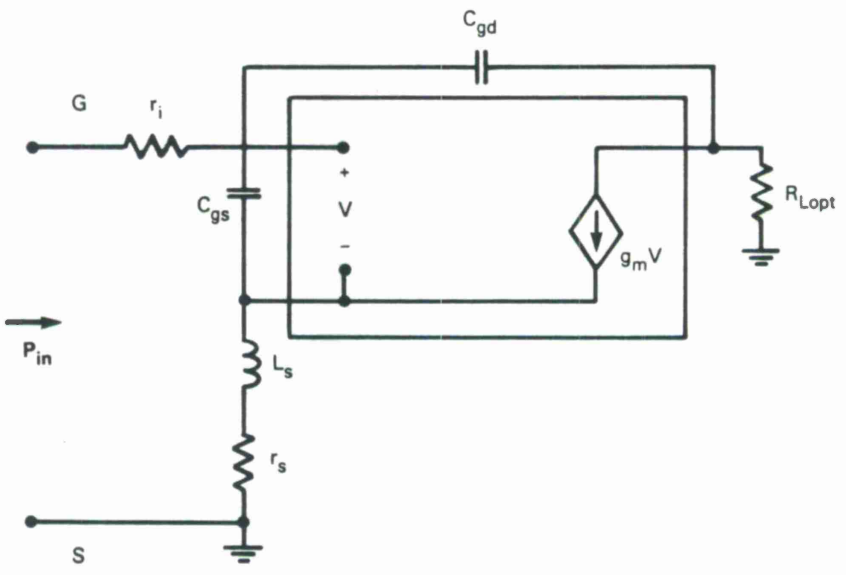
Having derived expressions for output power and efficiency, the one remaining piece of information needed to estimate power amplifier performance is large-signal gain, G. Since G is simply the ratio of output power to input power, and since output power has already been estimated, all that remains is to estimate input power. Section 3.1 deals with input power and gain calculation, while Section 3.2 examines the effect small-signal (incremental) output impedance has on G.

3.1 Input Power and Large-Signal Gain Calculation

This problem is broken down into two parts (Figure 3-1). For a given load circuit $Z_L[n]$, using the device dc I-V curves and the quasi-static analysis of Section 2, estimates of output power, drain efficiency, and input control voltage swing $|V|$ can be obtained [Figure 3-1(a)]. V is



(a)



(b)

103225-6

Figure 3-1. Large-signal gain calculation: (a) determining control voltage $|V|$ needed to produce P_{out}, and (b) determining P_{in} needed to produce $|V|$.

defined as the voltage across C_{gs}, and at dc it is equal to V_{GS}. All else being equal, the smaller the control voltage required to produce a given output waveform, the more gain a device will have. Having determined what $|V|$ is necessary to produce the desired output waveforms, the device small-signal model [Figure 3-1(b)] is employed to determine just how much input power is required to produce $|V|$. While this method provides a means to calculate G, it does not explicitly describe how to realize this gain in practice. Section 4 provides the answer, discussing matching-network design.

Before going any further, it is appropriate to justify some of the assumptions made in this approach. First, at what bias point should the small-signal model of Figure 3-1(b) be derived? While many of the parameters of the model (such as L_s and r_s) are independent of bias, other parameters (C_{gs} and C_{gd}) are somewhat sensitive to bias, and at least one parameter, g_m, can be very sensitive (in the linear-g_m case). Since g_m is used here in the input power calculation [Figure 3-1(b)], but not in the calculation of $|V|$ [Figure 3-1(a)], it turns out that the g_m influence on this calculation is not as important as one might think. Counterintuitively, it turns out that for this G calculation, to be conservative, the maximum small-signal g_m should be used. This is convenient, since most small-signal models are derived at the maximum small-signal gain bias point. In most PBTs and FETs, this high-g_m bias point also corresponds to the point of maximum C_{gs}, since high g_m's are usually obtained at high currents which, in turn, are obtained at zero or even slightly positive gate-to-source voltages. Again, this choice of parameter value (maximum C_{gs}) is the most conservative for this gain calculation. An alternative approach might be to take some kind of average component value, using either a simple-time or a state-space average (as employed in power supply design [8]).

Three simplifying assumptions concerning the output circuit are made in this approach:

(1) The device internal current source "sees" $Z_L[n]$ directly across it for the purposes of constructing the load-line [Figure 3-1(a)]. C_{ds} and any drain inductance have been absorbed into $Z_L[n]$.

(2) The small-signal output resistance r_{ds} is ignored.

(3) All the device output power is delivered to the load.

The first assumption neglects the common-lead inductance and resistance (L_s and r_s, respectively) in the output circuit calculations, which although not strictly valid, has been found to be reasonably accurate due to the other, larger impedances involved. In contrast, these common-lead impedances are included in the input-power calculations, since at high frequencies, all the other impedances in the input circuit are quite small. Turning to the second assumption, although no small-signal output resistance r_{ds} is explicitly included, as explained in Section 3.2 it has not been neglected. The third assumption states that any series output resistance r_d is negligible, output power dissipated in the common-lead resistance is also negligible, and that the device output is perfectly matched. This third assumption is one of the reasons this method fails to predict the observed drop in output power that occurs at the higher operating frequencies. (Other reasons, including transit time effects, have also been neglected.)

As stated above, the large-signal gain calculation procedure has two steps:

(1) Determine the device output power along with the magnitude of the control voltage $|V|$ needed to produce the output waveforms [Figure 3-1(a)] based on a load-line superimposed on the device static I-V curves.

(2) Calculate the input power P_{in} needed to produce $|V|$ across C_{gs} [Figure 3-1(b)].

The first step is straightforward once a load-line is known. (Load-lines were discussed a bit in Section 2 and will be discussed in greater detail in Section 4.)

The remainder of this section is devoted to the calculation of input power P_{in} needed to produce $|V|$. P_{in} can be calculated in a number of different ways, depending on the application and the accuracy needed. Device designers prefer closed-form expressions, so that the effects of varying a device parameter can easily be evaluated. Although circuit designers can also make use of closed-form expressions, increased accuracy and speed, as obtained from a computer simulation, are usually more important. Four different input-power calculations are presented below, from the simplest, least-accurate method to the most complex and most accurate. The first three methods derive closed-form expressions for P_{in} based on equivalent circuits, while the fourth determines P_{in} using a linear-CAD program (Super-Compact) along with a simple formula.

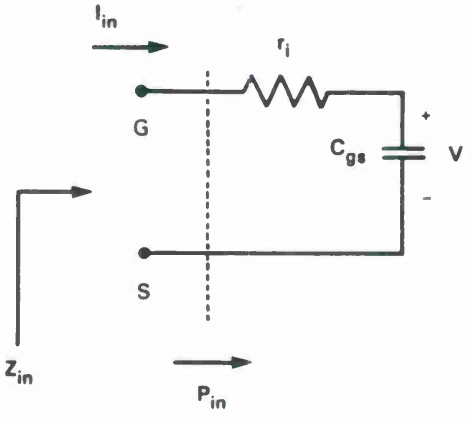
3.1.1 Closed-Form Expressions for Input Power

The first, and simplest, method to calculate P_{in} models the device input circuitry as a simple R-C network (Figure 3-2). This is the method used by Courtney and Gopinath [2] and is the basis for the other more complex and accurate methods proposed below. From basic circuit theory,

$$P_{in} = |I_{in}|^2_{rms} \, \mathrm{Re}\,\{Z_{in}\} \tag{3.1}$$

$$= \omega^2 \, C_{gs}^2 \, |V|^2_{rms} \, r_i$$

$$= 0.5 \, \omega^2 \, C_{gs}^2 \, |V|^2_{0\text{-}p} \, r_i \quad . \tag{3.2}$$



103226-8

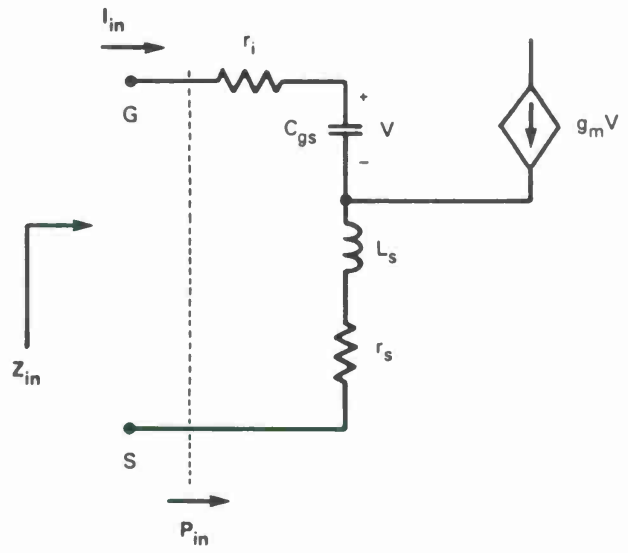
Figure 3-2. Simple device input model.

Although simple, Equation (3.2) shows some of the most important dependencies that are present in all the following results. In order to produce a given control voltage swing $|V|$, as frequency is increased input power must also be increased to make up for the shorting effect of C_{gs}. The commonly observed 6-dB/octave gain rolloff is obvious from this expression, since P_{in} goes as the square of frequency. The effect of scaling a device can also be seen from this equation. If the device size is doubled, C_{gs} will be doubled and r_i halved, resulting in twice the input-power requirement. Since doubling the device area also doubles I_{max}, output power will also be doubled, leaving large-signal gain unchanged, as expected.

Unfortunately, while simple, the above method is not very accurate. Using Equation (3.2) to estimate the large-signal gain of a 22-GHz, Class A PBT amplifier resulted in a drastically optimistic estimate of 17.9 dB, compared with a measured gain of just 6 dB. Clearly, this simple model is inadequate. By adding 3 more circuit-elements (Figure 3-3) — the common-lead inductance L_s, common-lead resistance r_s and controlled current-source $g_m V$ — much better accuracy is attained. Using Equation (3.1) to calculate the input power for this circuit results in

$$P_{in} = 0.5\ \omega^2\ C_{gs}^2\ |V|_{0\text{-}p}^2\ (r_i + r_s + g_m L_s / C_{gs}) \quad . \tag{3.3}$$

Equation (3.3) is the same as (3.2), except for the addition of the last two terms which raise the input power required (and, therefore, lower the gain). For the 22-GHz PBT amplifier mentioned above, Equation (3.3) results in a large-signal gain estimate of 9.6 dB — much closer to the actual measured gain, but still several decibels high. This result shows how important common-lead impedance is to device gain. The following example further illustrates this point.



103225-7

Figure 3-3. Device input model extended to include common-lead impedance.

Most of the early PBT mask sets have devices of various sizes, referred to as $1 \times 1/2$, 1×1, 1×2, and 2×2, where these numbers give relative device length and width. A 2×2 device has eight times the active area as a $1 \times 1/2$ device, so its I_{max} is eight times higher, giving it eight times the power-handling capability of the smaller device. Unfortunately, measurements of this 2×2 device have shown it to have much less gain than the $1 \times 1/2$ device, making it useless at 22 GHz. Since the PBT is such a compact device, power distribution problems (differential phase shifts, etc.) are thought to be negligible, so this problem which is common to power-FETs, does not explain the 2×2 PBT gain reduction. With the aid of Equation (3.3), the problem can easily be explained. Due to the geometry of these early PBTs, as the device size increases, all the device parameters scale as expected except for the common-lead inductance and resistance, which change only slightly [9]. In other words, for a device scaled by a factor n,

$$\begin{aligned} C_{gs} &\leftarrow n\, C_{gs} \\ g_m &\leftarrow n\, g_m \\ r_i &\leftarrow r_i/n \\ P_{out} &\leftarrow n\, P_{out} \end{aligned} \qquad \text{But:} \quad \left.\begin{aligned} r_s &\leftarrow r_s \\ L_s &\leftarrow L_s \end{aligned}\right\} \text{ do not scale}$$

since $G = P_{out}/P_{in}$, the ratio of the scaled device gain to that of the original device is given by

$$G_n/G_1 = \frac{P_{out\ n}/P_{in\ n}}{P_{out\ 1}/P_{in\ 1}} = \frac{P_{out\ n}}{P_{out\ 1}} \frac{P_{in\ 1}}{P_{in\ n}} \quad , \tag{3.4}$$

where the subscripts n and 1 represent the scaling factor. Plugging Equation (3.3) into (3.4) along with the above scaling relationships results in

$$G_n/G_1 = \frac{r_i + r_s + g_m\, L_s/C_{gs}}{r_i + n\,(r_s + g_m\, L_s/C_{gs})} \quad . \tag{3.5}$$

Table 3-1 contains the results of evaluating Equation (3.5) for the different size devices from an early PBT wafer. As can be seen, due to the common-lead impedance not scaling with the rest of the device, as the device-size increases, the gain decreases. Experimental results confirm this trend, although not by the exact amounts given in the table. A 1×1 device from this wafer had a 22-GHz Class A gain of about 7 dB, while a 2×2 device from the same wafer had a gain of -0.5 dB, a 7.5-dB drop (compared with a predicted drop of 4.9 dB). This additional measured gain drop may be due to excessive heating in the 2×2 device, since this early design was not optimized for high-power operation. The other thing to keep in mind is that this model is still rather simple, better suited to assess general trends than to predict exact performance.

TABLE 3-1

Gain Degradation in Scaled PBTs due to Fixed Common-Lead Impedance

Device Size	Scaling Factor (n)	G_n/G_1	G_n/G_1 (dB)
$1 \times 1/2$	1	1	0
1×1	2	0.65	-1.9
1×2	4	0.38	-4.2
2×2	8	0.21	-6.8

In order to make this model more complete, it would be nice to add the feedback capacitance, C_{gd}, to the circuit of Figure 3-3. Unfortunately, deriving a closed-form expression for Pin for this circuit becomes an algebraic nightmare. The effect of adding C_{gd} can be more easily assessed using the circuit of Figure 3-4(a), where the common-lead impedances have once again been neglected.

The analysis of Figure 3-4(a) is greatly simplified by first determining the equivalent impedance Z_{eq} of the right half of the circuit. After some basic circuit analysis, the same Z_{eq} can be obtained by replacing the controlled current source $g_m V$, C_{gd}, and R_L of Figure 3-4(a) with the series C-R combination (C_f, r_f) of Figure 3-4(b); C_f and r_f are seen to be C_{gd} and R_L, respectively, scaled down in impedance by the term $1 + g_m R_L$.

Using Equation (3.1) to calculate the input power for the circuit of Figure 3-4(b) results in

$$P_{in} = 0.5\ \omega^2\ C_{gs}^2\ |V|_{0\text{-}p}^2 \left\{ 1 + \frac{[1 + C_f/C_{gs}]^2 - 1}{1 + (\omega/\omega_1)^2} \right\} \left\{ r_i + \frac{r_f}{(1 + C_{gs}/C_f)^2\ [1 + (\omega/\omega_2)^2]} \right\} \tag{3.6}$$

where

$$\omega_1 = \frac{1}{C_f r_f} = \frac{1}{C_{gd} R_L} \quad ; \quad \omega_2 = \frac{1}{C' r_f} \quad ; \quad C' = \frac{1}{\frac{1}{C_{gs}} + \frac{1}{C_f}} \quad .$$

For $\omega << \omega_1 < \omega_2$, which is the usual case except at the highest operating frequencies (for the PBTs studied here, $\omega_1 \simeq 2\pi \times 90$ GHz), Equation (3.6) reduces to

$$P_{in} = 0.5\ \omega^2\ C_{gs}^2\ |V|_{0\text{-}p}^2\ (1 + C_f/C_{gs})^2 \left[r_i + \frac{r_f}{(1 + C_{gs}/C_f)^2} \right] \tag{3.7}$$

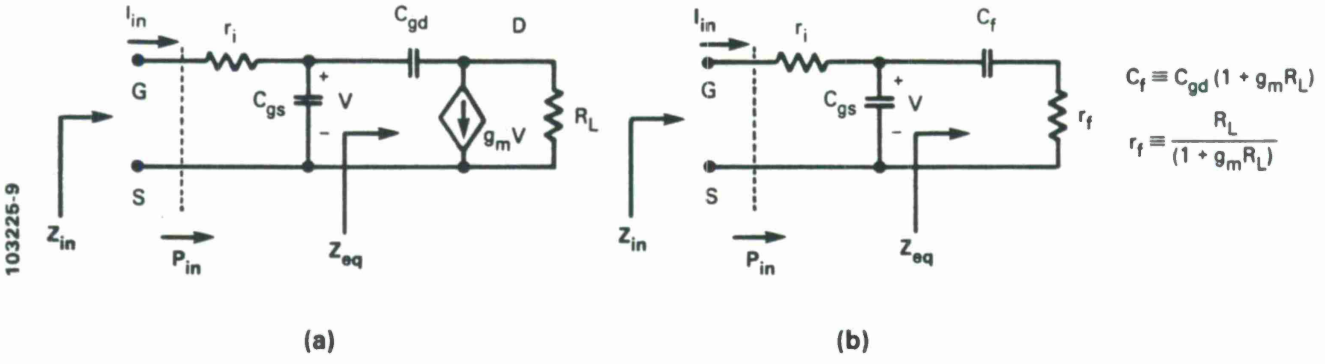


Figure 3-4. Device input model extended to include feedback capacitance: (a) original and (b) equivalent models.

As expected, the P_{in} required when C_{gd} is present [Equation (3.7)] is greater than when it is absent [Equation (3.2)], resulting in a decrease in gain. Equation (3.7) reduces to (3.2) if C_{gd} (and therefore C_f) is made zero.

If Equation (3.7) is used to predict the large-signal gain of the 22-GHz, Class A PBT power amplifier, an overly optimistic estimate of 12.5 dB results. Once again, these simplistic closed-form solutions are good for examining relationships between parameters, but do not provide an accurate enough estimate for predicting circuit performance. What is needed is a method that allows all the device parasitics to be included simultaneously. As mentioned above, finding closed-form solutions when more than a few reactive components are present becomes quite painful. A computer is much better suited to this analysis task.

3.1.2 A Fast and Simple Computer-Aided Method of Calculating Input Power

As mentioned in the Introduction, nonlinear-CAD programs that can analyze power amplifier circuits are now available, but they are computation-intensive due to their analysis methods. Additionally, due both to their expense and the fact that they are relatively new, far fewer microwave engineers have access to these nonlinear programs compared to those having access to linear-CAD programs. The method below is a simple, yet accurate method of determining power amplifier input power P_{in} using a linear-CAD program. Combining these results with the output power estimates of Section 2 gives a good approximation to large-signal gain. Although Super-Compact is used in the example, the method is easily adapted for other programs. As stated earlier, even those designers having access to a harmonic-balance simulator may still find this method useful to determine initial conditions for those iterative procedures.

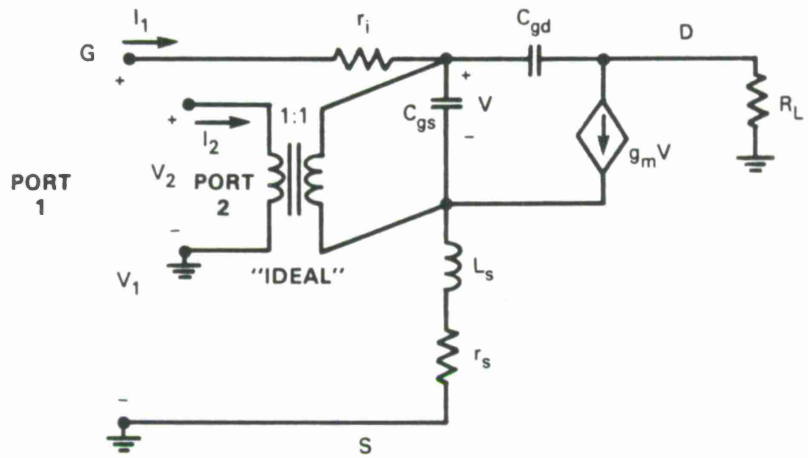
Once again, this method starts from Equation (3.1), repeated below for convenience:

$$P_{in} = |I_{in}|^2_{rms}\ \mathrm{Re}\{Z_{in}\} = 0.5\ |I_{in}|^2_{0\text{-}p}\ \mathrm{Re}\{Z_{in}\}$$

Z_{in} is easily found for a transistor input network using a linear-CAD program. All that remains is to determine the relationship between I_{in} and $|V|$, the control voltage, as was done in the closed-form solutions above. Equation (3.1) can be rewritten as

$$P_{in} = 0.5\ |V|^2_{0\text{-}p}\left(\frac{|I_{in}|^2_{0\text{-}p}}{|V|^2_{0\text{-}p}}\right)\mathrm{Re}\ \{Z_{in}\} \quad . \tag{3.8}$$

If a linear-CAD program could be made to evaluate the transadmittance term $|I_{in}|^2/|V|^2$ above, a solution would be in hand. Super-Compact Version 1.81 was used for this analysis and did not allow this term to be evaluated directly, but it was "tricked" into calculating it with the aid of an added "ideal" transformer, as shown Figure 3-5. This is the full input circuit of the transistor, including common-lead inductance, resistance, and feedback capacitance, along with an



103225-10

Figure 3-5. Device input model with 1:1 transformer added for CAD analysis.

ideal 1:1 transformer across the gate-source capacitance. This transformer is needed to access the floating (relative to ground) control voltage V, since Super-Compact requires that one terminal of every port be at ground potential. A 2-port network is formed, with the ports as labeled. Although a transadmittance is needed for Equation (3.8), the 2-port Z-, not Y-parameters, should be employed to avoid loading the circuit. This is understood by comparing the definitions of Z-to Y-parameters:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \quad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad . \tag{3.9}$$

Since the relationship between I_1 (I_{in}) and V_2 (V) is desired, only Z_{21} or Y_{12} could contain the needed information. By examining these definitions, it becomes clear that Z_{21} is the parameter to use:

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2 = 0} \quad , \qquad Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1 = 0} \quad . \tag{3.10}$$

Z_{21} is the ratio of V_2 to I_1 with an open circuit at port 2 (i.e., no loading), whereas Y_{12} is the ratio of I_1 to V_2 with a short circuit at port 1 (i.e., severe loading).*

Equation (3.8) can be rewritten in terms of the circuit Z-parameters (remember that port 2 for this calculation is across the ideal transformer, not across the device drain-source terminals):

$$P_{in} = 0.5\ |V|^2_{0\text{-}p} \quad \frac{1}{|Z_{21}|^2} \quad \mathrm{Re}\left\{Z_{11}\right\} \quad . \tag{3.11}$$

After analyzing the circuit of Figure 3-5 with Super-Compact, the user is required to manually plug the results (Z_{11} and Z_{21}), along with $|V|_{0\text{-}p}$ (determined from the load-line) into Equation (3.11) to get input power. This result, combined with an output power estimate from Section 2, determines large-signal gain. Using this method on the 22-GHz PBT amplifier discussed above results in a large-signal gain estimate of 7.2 dB, fairly close to the measured 6-dB gain. The remaining discrepancy can be explained by the fact that the small-signal model used was actually derived from S-parameter data taken on a device from a similar, but slightly higher-gain wafer. When this method is applied to a more accurately modeled device, the results are even better (see Section 4.

3.2 Effect of Small-Signal Output Impedance on Large-Signal Gain

One of the assumptions made in Section 3.1, was that the small-signal output impedance r_{ds} could be ignored, however this section briefly shows that r_{ds} was implicitly included in the above analysis. Further, it is shown that r_{ds} has little effect on device output power, but can degrade large-signal gain significantly.

As was shown in Section 2, the rf output power of a device is determined by the $\Delta I \cdot \Delta V$ product, as determined from the load-line. If the output resistance r_{ds} is reduced from infinity to a value comparable to the load resistance R_L, the output voltage and current swings will be reduced, reducing output power. However, by increasing the amplitude and changing the dc

---

* For the reader who is still unconvinced that Y_{12} will not work, calculating the Z- and Y-parameters for the simple case of the R-C input network of Figure 6 should do the trick. For this circuit, $Y_{12} = -1/r_i$, while $1/Z_{21} = sC_{gs}$. Plugging these relationships into Equation (3.8) for the current/voltage ratio results in the correct input-power expression [Equation (3.2)] only if $1/Z_{21}$ is used.

offset of the gate-voltage drive waveform, the original drain-source voltage and current waveforms can be restored, restoring output power to its original value, as illustrated in Figure 3-6. A Class A amplifier with a constant-g_m device is assumed. For convenience, the device is also assumed to have a finite incremental output resistance r_{ds} equal to the load resistance R_L. The input control characteristic (I_{DS} versus V_{GS}) is no longer a single curve, but a family of curves, with V_{DS} as a parameter.

Consider what happens when this device is driven with the standard Class A gate-source drive waveform (labeled "$r_{ds} = \infty$"). During the most positive portion of the gate-voltage swing ($v_{GS} \simeq 0$), the finite output impedance has little effect. In contrast, when the gate voltage swings down to V_P, instead of pinching-off as in the infinite output-impedance case, the device still allows a current flow of $I_{max}/2$. Although not explicitly drawn in this figure, the drain-source current and voltage swings have both been reduced by a factor of 2, reducing the output power by 6 dB.

By doubling the amplitude and dc offset of the original gate-drive waveform (resulting in the waveform labeled "$r_{ds} = R_L$"), the original output voltage and current waveforms can be restored. The price paid is a 6-dB drop in gain, but at least the output power is now the same as in the infinite-r_{ds} case. Note that the gate control characteristic in this case has half its original slope, so the effective g_m is half what it was with $r_{ds} = \infty$. While quantitative expressions can be derived for the gain-drop expected for other values of r_{ds} and R_L, these derivations will not be included. Instead, by looking at the gate voltages along an amplifier load-line, the required input-control voltage swing $|V|$ is immediately apparent. Any decrease in r_{ds} manifests itself in an increase in $|V|$ needed to achieve the desired output waveforms, increasing the input power required and decreasing the large-signal gain.

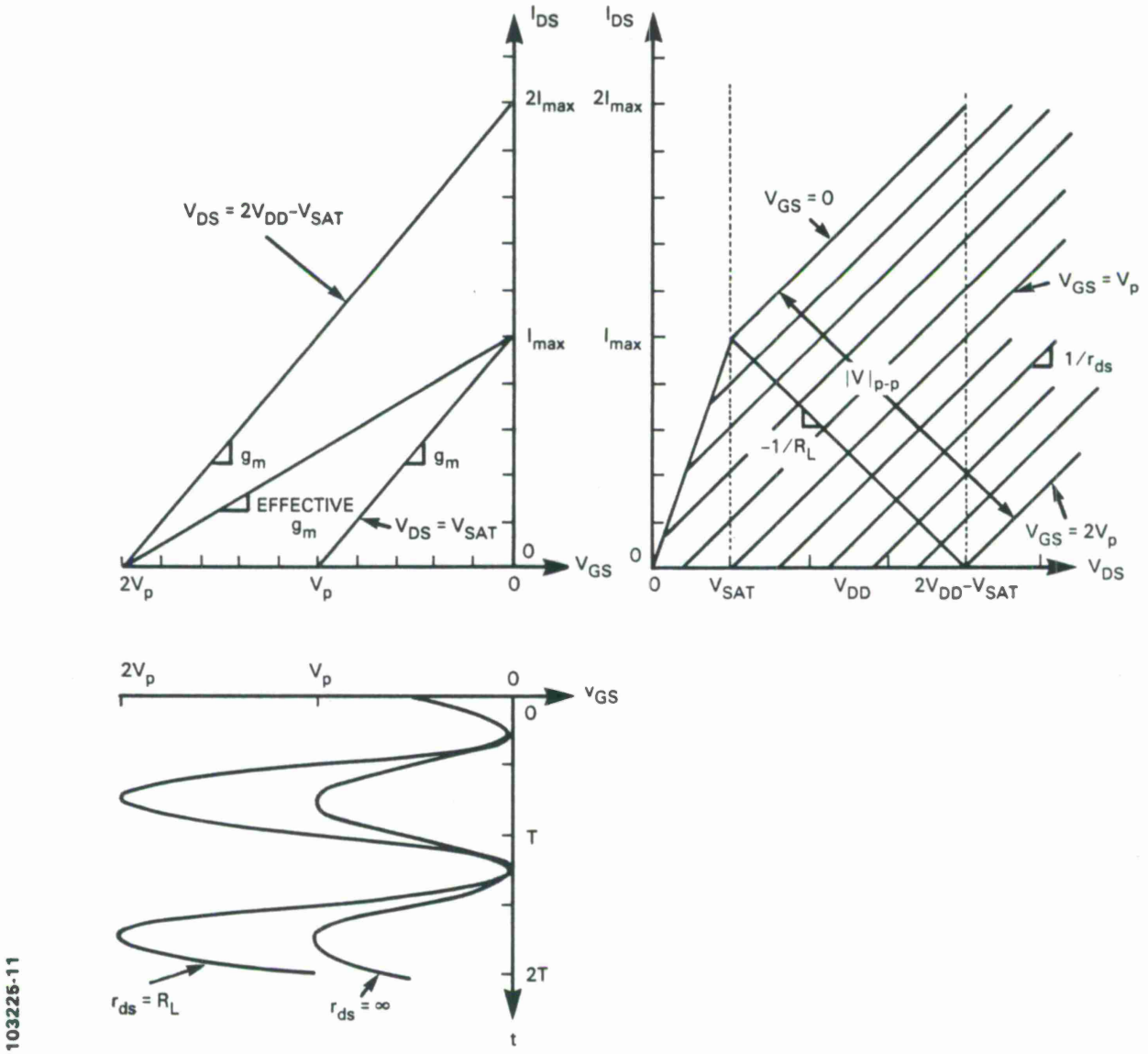


Figure 3-6. Effect of finite output impedance.

4. LOAD-LINE SELECTION AND MATCHING NETWORK DESIGN

In this section, previous results are brought together to form a simple power amplifier design procedure of three basic steps: load-line selection, matching network design, and performance estimation. A different example of a 22-GHz Class A PBT power amplifier is used to illustrate this method.

4.1 Load-Line Selection

This section elaborates on the load-line selection process discussed in Section 2. Selecting the load-line is undoubtedly the most important step in the design process. The load-line determines output power and drain efficiency and is the primary determinant of large-signal gain. Selection of the output circuitry and the device bias point determines which load-line is traversed.

Tables 2-2 and 2-3 give the optimum load resistance R_{Lopt} for the various device and amplifier types. As discussed in Section 2, this optimum load resistance was selected to maximize device output power. Load resistances greater than R_{Lopt} result in reduced current swing ΔI, while resistances less than R_{Lopt} result in reduced voltage swing ΔV.

From the discussion in Section 2, it is clear that one end of all the load-lines should be at the point (V_{SAT}, I_{max}). At this end, the device has large small-signal gain, due to the wide spacing between the device curves.* The other end of the load-line will be on the x-axis (zero current); the exact location of this voltage intercept point depends on the supply voltage, amplifier class, and device type, as illustrated in Figure 4-1. Note that while all the amplifiers employing a tuned-load circuit swing from V_{SAT} to $2V_{DD} - V_{SAT}$, most of the resistively loaded amplifiers have a reduced voltage swing. Due to energy storage in their tank circuits, the tuned Class B amplifiers all have load-lines that hit the x-axis at (V_{DD}, 0) and continue to increase along this voltage axis even though their drain-source current is zero. In contrast, without a tank circuit the drain-source voltage of the resistively loaded Class B amplifiers cannot change when drain-source current is zero.

Selection of the supply voltage V_{DD} is not quite as straightforward as one may think. If the device dc I-V curves remain equally spaced as drain-source voltage is increased, and if the device can handle the power dissipation, then V_{DD} can be set equal to the V_{DDmax} values given in Table 2-3 to get maximum output power. On the other hand, if the spacing between the dc I-V curves becomes reduced at higher voltages (this has been the case for most of the early PBTs that have been measured), then operating at higher supply voltages will result in a reduction of large-signal gain. Additionally, due to power-dissipation limits, operating at V_{DDmax} may not always be possible. This is especially true in Class A operation, since with no rf signal applied, power dissipation is quite high.

---

* While this is true for PBTs and most FETs, this may not be true for HEMTs which have maximum curve spacing at lower currents.

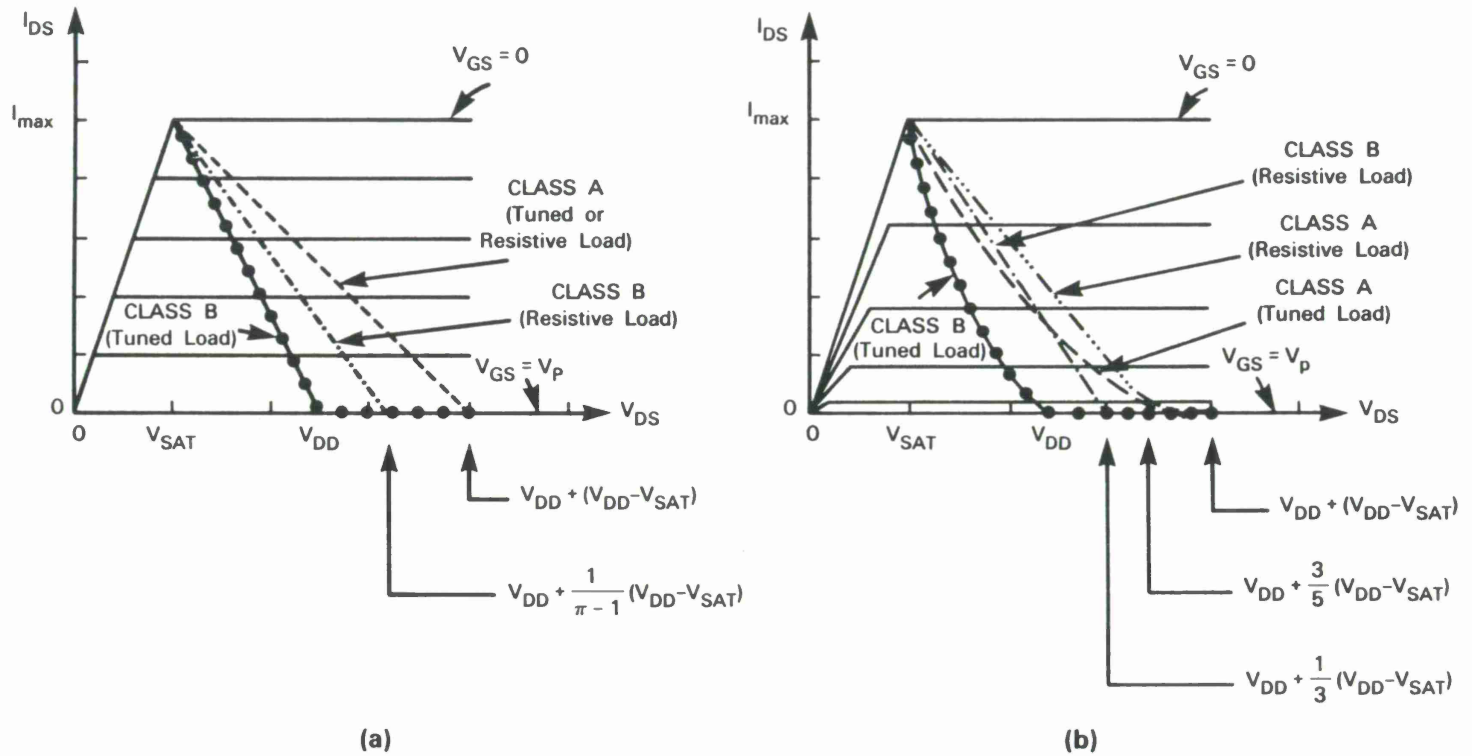


Figure 4-1. Load-lines: (a) constant- and (b) linear-g_m devices.

103225-12

Figure 4-2 shows the dc I-V curves for a different PBT (a 1 × 1 device from the wafer 2P23A) from the one used in the prior examples. Notice that the device curves are spaced far apart at low drain-source voltage and high currents, but group much closer together for higher voltages and lower currents. While a curve is plotted for V_{GS} = 0.7, this curve will be avoided since a fair amount of gate current is drawn at this bias point due to the gate-source junction turning on. For this device, $I_{max} \simeq 120$ mA and $V_{SAT} \simeq 1.8$ V.

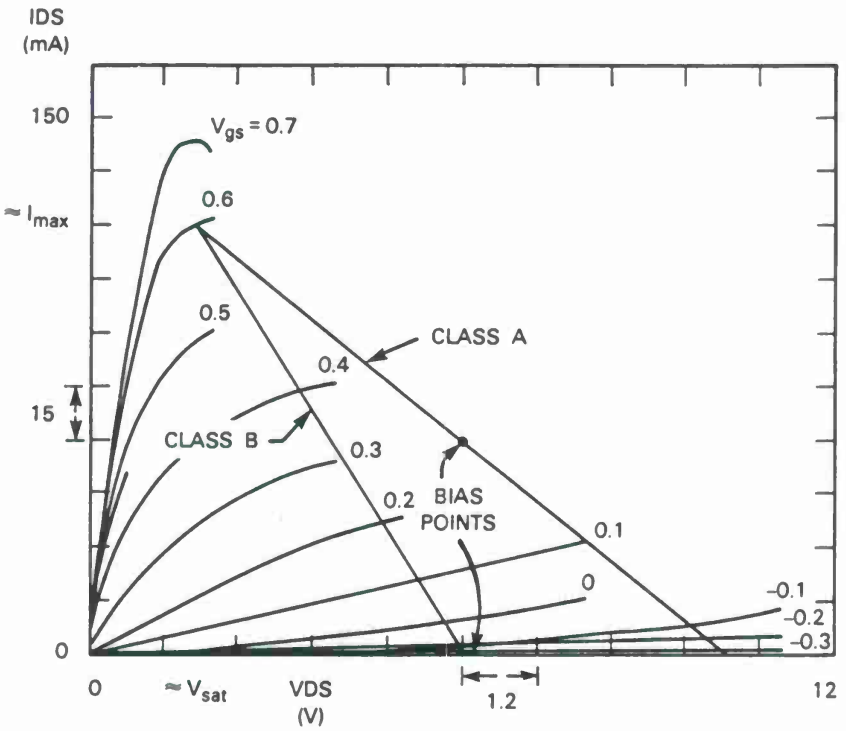


Figure 4-2. PBT I-V characteristics and load-lines (wafer 2P23A, 1 × 1 device).

Assuming that a tuned load is used, approximate Class A and B load-lines can be drawn in. As stated earlier, tuned loads (i.e., shorting all the harmonics) result in better efficiencies, so they should be employed whenever feasible. For this example, V_{DD} = 6 V was selected as a bias voltage, as a reasonable compromise between output power, gain, and dissipation. Note that these load-lines are only approximate, since the PBT is not really a constant- or linear-g_m device, but somewhere in between. As seen in Figure 4-1, as long as tuned loads are used, the constant- and linear-g_m device load-lines begin and end at the same points, but have different shapes (straight or curved). As far as the gain analysis is concerned, this shape difference has little effect. What is really important is how much gate-control voltage swing |V| is needed to get the desired output waveforms. From Figure 4-2, for this PBT operating Class A, ~ 0.9 V peak-to-peak (0.6 to

–0.3 V) is needed, while in Class B, ~ 0.7 V zero-to-peak (0.6 to –0.1 V) is needed. Note that if the I-V curves were perfectly flat, the Class B amplifier would require twice the gate-control voltage swing as the Class A amplifier, as expected, since half the Class B gate-voltage swing must produce the entire current swing.

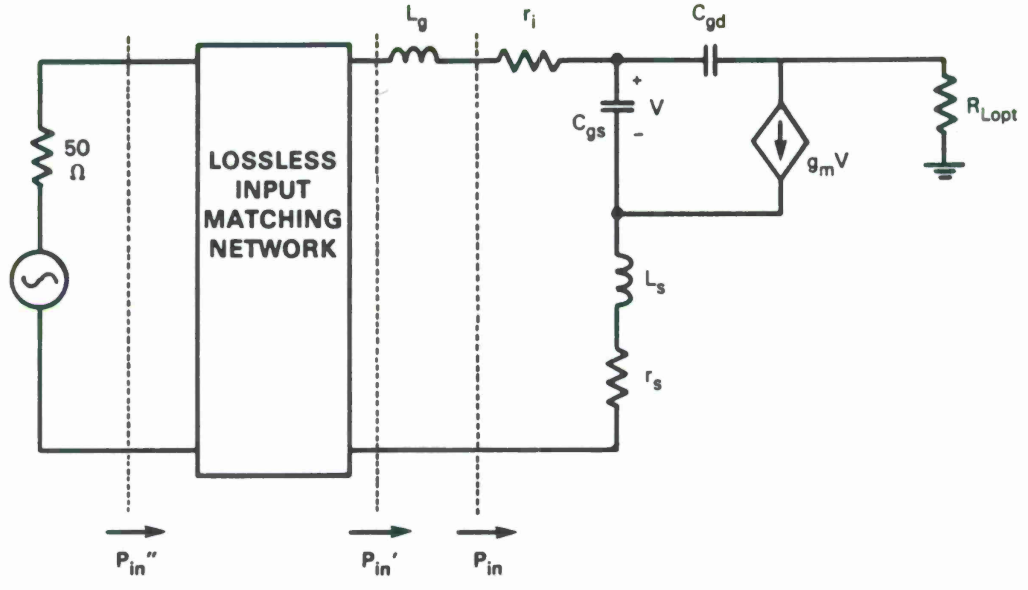
4.2 Matching Network Design

The previous sections described how to produce the desired output power P_{out} from a device by selecting a load-line and driving it with the proper control voltage waveform. This control voltage, in turn, is determined by the input power P_{in}, the gate bias point, and the device input equivalent circuit. This section gives a simple method of designing the matching networks needed to present the required R_{Lopt} to the device output, and to deliver P_{in} to the device input. Figure 4-3 summarizes the problem statement. Between the 50-Ω input signal generator and the device input is a lossless input matching network and a wire-bond (or mesh) inductance L_g [Figure 4-3(a)]. Similarly, between the device-controlled current source and the 50-Ω load resistor is the device drain-source capacitance C_{ds}, a bonding inductance L_d, and a lossless output matching network [Figure 4-3(b)]. Since the input and output matching networks are assumed to be lossless, $P_{in}'' = P_{in}' = P_{in}$ and $P_{out}'' = P_{out}' = P_{out}$. Thus, the matching networks and device parasitics perform lossless impedance transformations from the 50-Ω system to the internal device level.

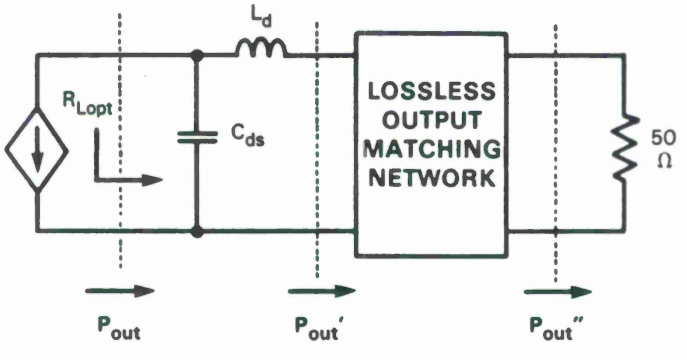
The input matching network can be designed in the same manner as in a small-signal amplifier, conjugate-matching the device input impedance for maximum power transfer. The output matching is also similar to the small-signal case, but instead of presenting the device current source with a real impedance equal to r_{ds}, the output circuitry should present an impedance of R_{Lopt}. The output matching network can be designed by starting with a fictitious resistance (equal to R_{Lopt}) "down" in the device across the current source, and working backwards out towards the 50-Ω load.

This procedure is illustrated in Figure 4-4(a) for the new 22-GHz Class A PBT amplifier example. From Table 2-2, $R_{Lopt} \simeq 2(V_{DD} - V_{SAT})I_{max}$. From the device I-V curves of Figure 4-2, $V_{SAT} \simeq 1.8$ V, $I_{max} \simeq 120$ mA, so at 6-V bias, $R_{Lopt} \simeq 2(6 - 1.8)/0.12 = 70$ Ω. Starting at 70 Ω (point A), C_{ds} moves the impedance along a constant-conductance circle, followed by the series inductance L_d which moves the impedance up the constant-resistance circle to point B. A simple output matching network consisting of a series 50-Ω transmission lines rotating the impedance around to the real axis (point C), and a quarter-wave transformer bringing the impedance up to 50 Ω (point D), completes the matching.

One important point neglected until now is stability. As in the case of small-signal amplifier design, stability circles can be calculated, and regions of instability avoided. Since the above procedure presents R_{Lopt} to the device instead of r_{ds}, the device is not really simultaneously conjugate-matched, so even if the stability factor k is less than unity, the above method could still result in a stable solution.



(a)



(b)

103225-14

Figure 4-3. Matching circuits: (a) input and (b) output.

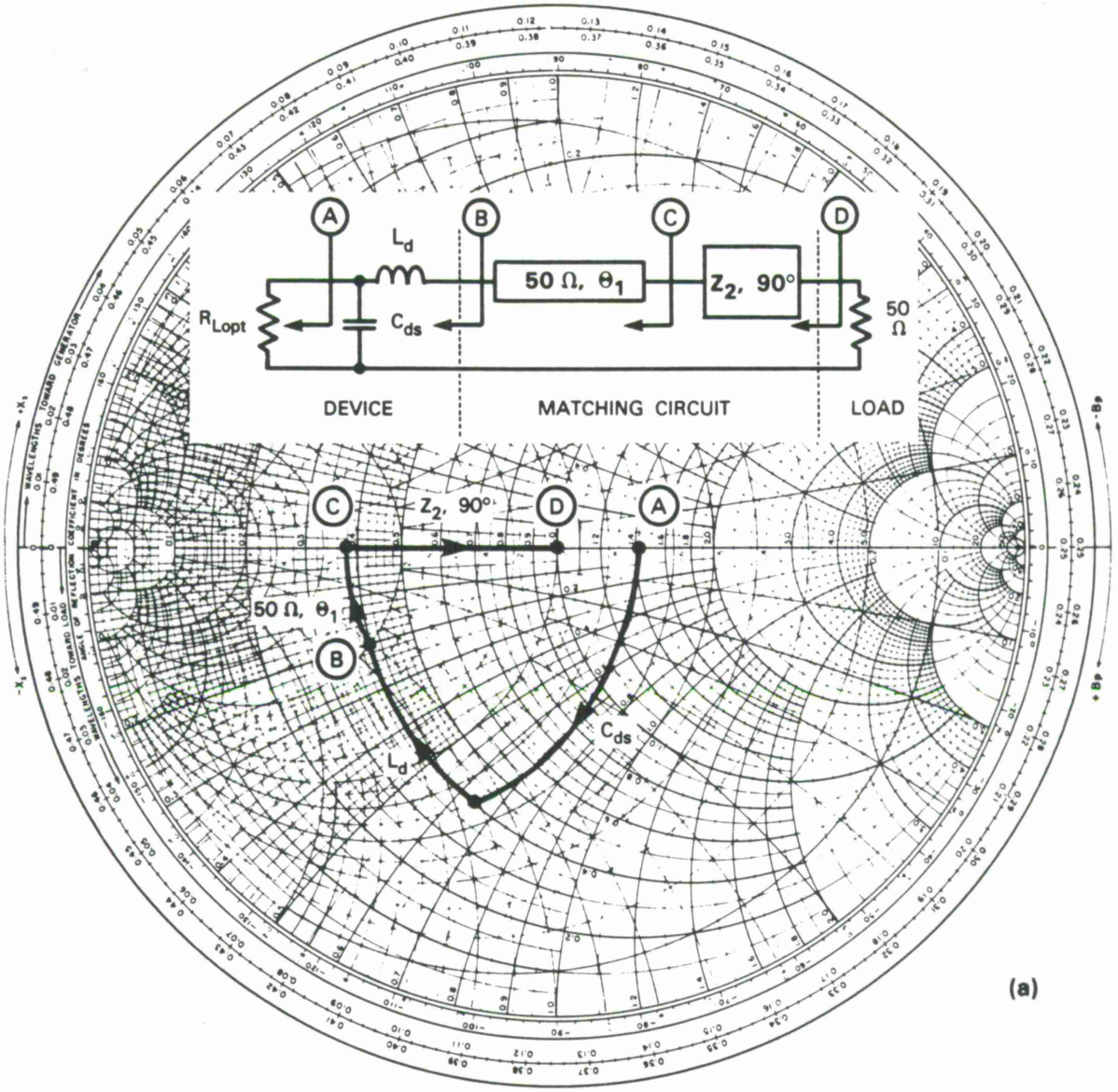
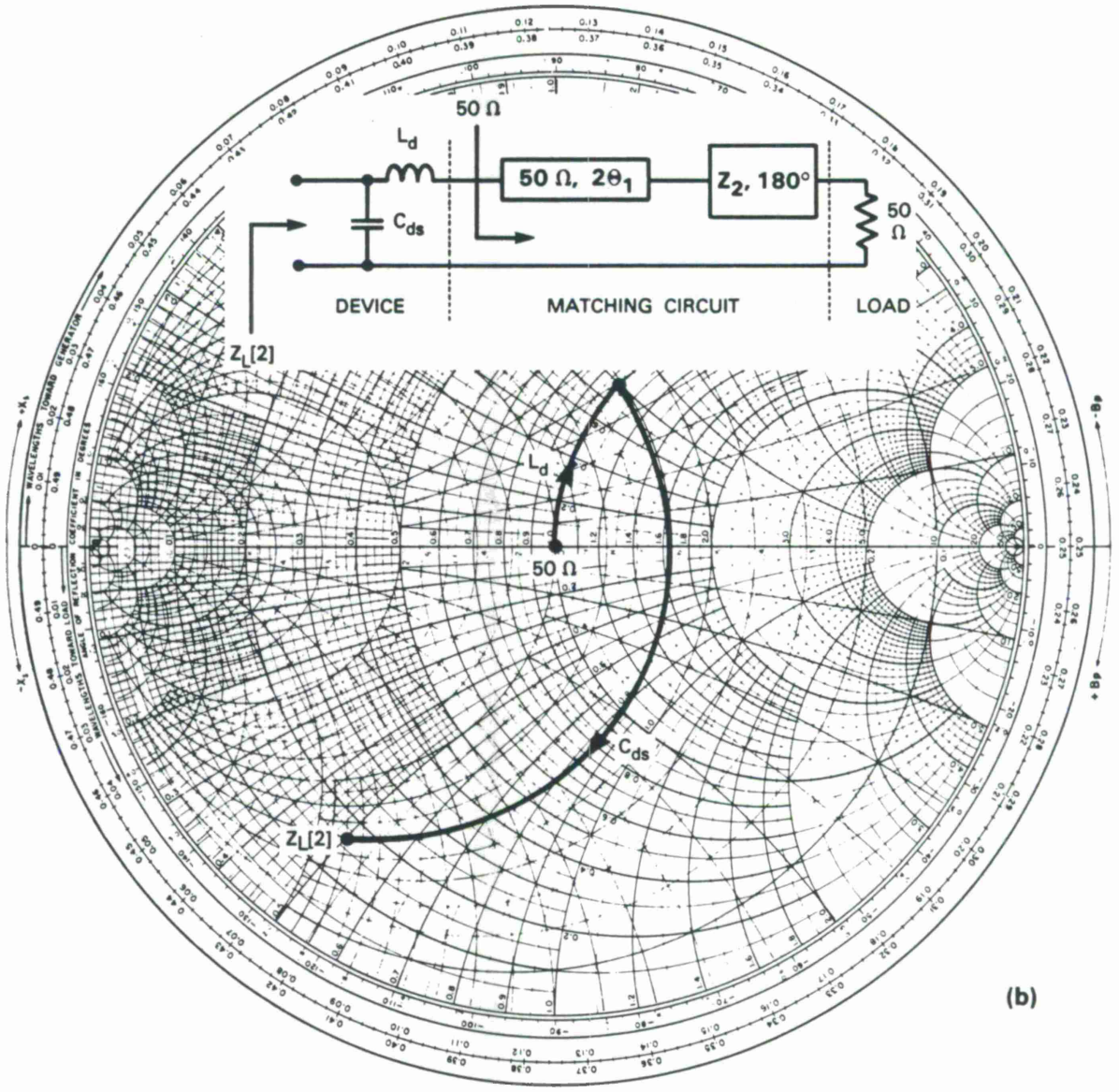


Figure 4-4(a). PBT amplifier output matching circuit: fundamental-frequency (22-GHz) design.



103226-16

Figure 4-4(b). PBT amplifier output matching circuit: second-harmonic (44-GHz) impedance.

This simple-minded matching circuit made no explicit attempt to terminate the harmonics (44, 66, 88 GHz, etc.) in a short circuit, but due to the shorting effect of C_{ds} at these high frequencies, a fairly low impedance is presented, as illustrated in Figure 4-4(b) for the second harmonic. Note that this harmonic-impedance analysis is approximate at best, since transmission-line dispersion and moding were neglected, and the load impedance is still presumed to be a perfect 50 Ω at 44 GHz. The higher-order harmonic frequencies will see still lower impedances, as the susceptance of C_{ds} increases with increasing frequency.

4.3 Large-Signal Performance Estimation and Verification

This section predicts the large-signal performance of the amplifier discussed above and compares these predictions to measured performance. The results are quite good, given the approximate nature of this method. This procedure has been repeated many other times on various devices, yielding consistently good results.

As shown in Table 2-2, for the Class A PBT amplifier biased at 6 V, 60 mA,

$$P_{out} = (V_{DD} - V_{SAT})\, I_{max}/4 = (6 - 1.8)\, 0.12/4 = 126 \text{ mW (21 dBm)}.$$

If the PBT were a constant-g_m device,

$$\text{drain efficiency} = \eta_D = 0.5\, (V_{DD} - V_{SAT})/V_{DD} = 0.5\, (6 - 1.8)/6 = 0.35 \text{ (i.e., 35 percent)},$$

whereas if it were a linear-g_m device,

$$\eta_D = 0.67\, (V_{DD} - V_{SAT})/V_{DD} = 0.67\, (6 - 1.8)/6 = 0.47 \text{ (i.e., 47 percent)}.$$

Large-signal gain was calculated using the approach of Section 3.1.2 (using Super-Compact to calculate the Z-parameters of the input network/ideal transformer combination). From the load-line of Figure 4-2, $|V|_{0\text{-}p} = 0.45$, and from Super-Compact, $|Z_{21}| = 3.36$, $\{\text{Re } Z_{11}\} = 2.43$. Using Equation (3.11), $P_{in} = 22$ mW (13.4 dBm), so the amplifier has a large-signal gain of 7.6 dB.

This amplifier was built using the output matching network of Figure 4-4(a) along with a simple circuit to conjugate-match the input. Testing in the lab was performed on a large-signal scalar network analyzer. Some slight (empirical) fine-tuning was needed to peak-up the response at 22 GHz, as would be expected given the mediocre return loss of the coaxial connectors and bias-tees used at these frequencies. Measured results compared quite favorably to the predicted values. Biased at 6 V, 60 mA, with an input drive level of 13.4 dBm, P_{out} = 20.4 dBm, G = 7 dB, and η_D = 30.5 percent. In order to get the 21-dBm output power as predicted, the input drive had to be increased to 14.2 dBm, resulting in a gain of 6.8 dB and a drain efficiency of 35 percent. It should be noted that for a device with a transconductance this high, determining $|V|_{0\text{-}p}$ accurately from the load-line is critical for precise gain predictions (a 0.1-V error makes a big difference).

5. CONCLUSIONS

Textbook output power, efficiency, and power-dissipation expressions were derived for Class A and B power amplifiers, for devices having either constant or linear transconductance, and for resistive or tuned loads. These results differ considerably from the simple cases usually included in most texts. It was shown that failure to properly terminate amplifier harmonic frequencies can dramatically degrade performance.

Several methods of large-signal gain estimation were presented, all based on input-power calculation. Three closed-form expressions for input power were derived which give direct relationships between the various device parameters and the large-signal gain. A novel method of calculating input power with the aid of device I-V characteristics, a small-signal device model, and a linear-CAD program was presented. Excellent correlation between estimated and measured performance was demonstrated.

A simple method of designing large-signal amplifiers was presented and demonstrated on a 22-GHz PBT amplifier. This method can be used as a stand-alone procedure for many power amplifier designs, or as a starting-point in nonlinear-CAD-based designs and load-pull measurements.

One limitation of the above results is that they contain no mechanism for power rolloff with frequency, as is commonly encountered at the higher microwave and millimeter-wave frequencies. This limitation could be overcome by calculating how much attenuation there is from the device internal current generator out to the device drain-source terminals, including device series output resistance r_d and common-lead impedance r_s and L_s. Additionally, transit-time (τ) effects could be included. With this added complexity, however, one might be better off using the simplified procedure to arrive at a first-cut design, and following it up with a more accurate harmonic-balance analysis and optimization.

REFERENCES

1. H.L. Krauss, C.W. Bostian, and F.H. Raab, *Solid State Radio Engineering*, New York: John Wiley & Sons (1980), pp. 348-476.

2. W.E. Courtney and A. Gopinath, personal communication (1986).

3. G. Zhou, T. Curtis, and R. Chen, "GaAs Microwave MESFET with Extremely Low Distortion," *IEEE MTT-S Digest*, 569 (1987).

4. Y. Tajima and P.D. Miller, "Design of Broad-band Power GaAs FET Amplifiers," *IEEE Trans. Microwave Theory Tech.*, **MTT-32**, 261 (1984).

5. D.M. Snider, "A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier," *IEEE Trans. Electron Devices*, **ED-14**, 851 (1967), DDC AD-670764.

6. F.H. Raab, "FET Power Amplifier Boosts Transmitter Efficiency," *Electronics*, 122 (1976).

7. J.R. Lane and H.K. Hahn, "Microwave Class B Power Amplifier Investigation," Final Report, Westinghouse Defense and Electronics Center, Advanced Technology Division (1986).

8. R.D. Middlebrook and S. Ćuk, "General Unified Approach to Modelling Switching-Converter Power Stages," *IEEE PESC Record*, 18 (1976).

9. Conversations with M.A. Hollis and R.H. Mathews, Lincoln Laboratory, MIT (1988).

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) Technical Report 812	5. MONITORING ORGANIZATION REPORT NUMBER(S) ESD-TR-88-181
6a. NAME OF PERFORMING ORGANIZATION Lincoln Laboratory, MIT 6b. OFFICE SYMBOL *(If applicable)*	7a. NAME OF MONITORING ORGANIZATION Electronic Systems Division
6c. ADDRESS *(City, State, and Zip Code)* P.O. Box 73 Lexington, MA 02173-0073	7b. ADDRESS *(City, State, and Zip Code)* Hanscom AFB, MA 01731
8a. NAME OF FUNDING/SPONSORING ORGANIZATION US Army, SATCOMA 8b. OFFICE SYMBOL *(If applicable)* AMCPM-SC-11	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F19628-85-C-0002
8c. ADDRESS *(City, State, and Zip Code)* Fort Monmouth, NJ 07703	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. 35314A; PROJECT NO. 585; TASK NO.; WORK UNIT ACCESSION NO.
11. TITLE *(Include Security Classification)* Microwave Power Amplifier Analysis and Design	
12. PERSONAL AUTHOR(S) Lawrence J. Kushner	
13a. TYPE OF REPORT Technical Report 13b. TIME COVERED FROM _____ TO _____	14. DATE OF REPORT *(Year, Month, Day)* 1988, December 16 15. PAGE COUNT 54
16. SUPPLEMENTARY NOTATION None	

17. COSATI CODES			18. SUBJECT TERMS *(Continue on reverse if necessary and identify by block number)*
FIELD	GROUP	SUB-GROUP	power amplifier, Class A, Class B; linear transconductance; harmonic termination; load-line; nonlinear CAD; constant transconductance; large-signal gain

19. ABSTRACT *(Continue on reverse if necessary and identify by block number)*

Output power, efficiency, power dissipation, and optimum load-resistance expressions for idealized microwave Class A and B power amplifiers are derived based on a waveform analysis. The effects of device transconductance variation with bias and circuit harmonic termination are examined. Large-signal gain is determined by calculating the input power needed to produce a given output power. Both closed-form and CAD-based solutions are presented, all based on device dc I-V characteristics and small-signal models. A practical power amplifier design procedure is given and used to design a 22-GHz permeable-base transistor (PBT) power amplifier. Although the analysis and design results presented here are useful by themselves, they are also intended to be used in conjunction with other CAD and measurement techniques (such as harmonic balance and load pull) to arrive at a starting point. Device designers also should find these results useful, allowing them to predict how changes in device parameters will affect microwave power amplifier performance.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT ☐ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION Unclassified
22a. NAME OF RESPONSIBLE INDIVIDUAL Lt. Col. Hugh L. Southall, USAF	22b. TELEPHONE *(Include Area Code)* (617) 981-2330 22c. OFFICE SYMBOL ESD/TML